Honeywell Level 6
Minicomputer Handbook

Honeywell

LEVEL 6 MINICOMPUTER
HANDBOOK

SERIES 60 (LEVEL 6)

SUBJECT:

Overview of System Components, Architecture, and Software; Programmer-oriented Discussion of
Instruction Set and Peripherals; Site Preparation Planning

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PREFACE

This Handbook introduces Level 6, Honeywell's new minicomputer system. It describes every major element of this system in straightforward technical detail. Thus present minicomputer users and others with an engineering orientation will come to understand the fundamental design philosophy of Level 6 and on this basis will be able to make a firm personal evaluation of its merits. They will also become reacquainted with Honeywell as a minicomputer manufacturer.

Honeywell has been a minicomputer manufacturer for 10 years. In that time it has marketed the products of Computer Control Company, which it acquired in 1966, and has developed and introduced extensions of the original line. Computer Control Company built one of the first 16-bit minicomputers, the DDP-116, in 1965. Honeywell has continued with the DDP-516 (1966), the DDP-416 (1967), the H316 (1969), and System 700 (1972), establishing itself as one of the foremost manufacturers of 16-bit systems.

Level 6 is a 16-bit minicomputer system founded on new concepts of simplicity, flexibility, and reliability. With its open-ended system architecture, its modular, highly functional software, and its low-cost peripherals (including diskettes), Level 6 presages a family of machines with wide-ranging suitability for both end-use and OEM applications. And as a partner with Honeywell's new Series 60 and a member of The Honeywell Information System, Level 6 enjoys the full field engineering service of one of the country's major computer manufacturers.

The heart of Level 6 is the Megabus, expandable to 23 slots — each with multiple device capability (diskettes, printers, card readers, communication controllers, etc.). Modularity has reached new levels, with implementation of an entire central processor or up to 32,768 words of memory on a single circuit board. Indeed, a complete minisystem of five boards (central processor, memory, and device and communication controllers), plus power supply, air circulating unit, and control panel, fits into a standard drawer 5¼ inches high.

Lying behind the advanced technology of Level 6 are not only Honeywell's long experience as a producer of 16-bit machines but a design philosophy emphasizing the use of commercially established elements and a new factory system promoting error-reducing automated procedures. These have combined to lower manufacturing costs to the point at which Level 6 can offer one of the most attractive cost/performance ratios on the market.

There is much more that is newsworthy about Level 6, and this Handbook can only summarize key aspects. For a full account of Honeywell's new minicomputer and its place in your operations, call a Honeywell Marketing Representative today.

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SECTION 1

SYSTEM SUMMARY

Level 6 engineering is highly contemporary, beginning with a Megabus permitting high-speed asynchronous data transfer and continuing with MOS memory, circuit boards of unusual capability, an extensive use of microprocessors, a large number of program-visible registers, a very large addressing capability, and an instruction set designed for extremely efficient programming. These and other aspects of Level 6 are described briefly in this section of the handbook and taken up in detail in the sections which follow. Table 1-1 provides a summary view of Level 6 components.

MODELS

Three models are presently available: the 6/06, the 6/34, and the 6/36. Model 6/06 is designed for end users, including present users of System 700. In addition to its Level 6 characteristics, Model 6/06 is compatible with System 700, allowing users to operate OS/700 software and DMA peripherals while taking advantage of the large capacity of the Megabus. Model 6/06 is documented extensively (see the Model 6/06 Programmer's Reference Manual, Order No. AT25) and will not be treated in this handbook.

Model 6/34 includes a central processor mounted in a four-slot Megabus chassis, a memory controller with parity, and an 8192-word MOS Memory-Pac (module). The central processor and maximum memory (32,768 words, in modules of 8192 words) each require only one circuit board. Up to four boards can be included in Model 6/34; thus after the CP and memory boards are plugged in, two boards are still available for the attachment of multiple peripheral devices and/or communication lines. The new, extremely economical Level 6 power supply (including an air circulating unit), a Basic Control Panel, multiply/divide hardware, a realtime clock, and a ROM bootstrap loader are included in this model. All software and peripherals listed in Table 1-1 are available.

TABLE 1-1. SUMMARY OF LEVEL 6
COMPONENTS

Level 6 Megabus	Provides bidirectional asynchronous communications path between all boards
Cycle Time:	300 nanoseconds
Throughput:	Up to 3 million words per second
Slots:	Up to four on Model 6/34; up to 23 on Model 6/36
Central Processor	Interrupt-driven; processes bits, bytes, words, and multiwords; real-time clock; ROM bootstrap loader; Basic (Model 6/34) or Full (Model 6/36) Control Panel; multiply/divide hardware
Instructions:	107
Addressing modes:	Direct (to up to 64K words); indirect; base plus displacement; base plus displacement indirect; base plus index; base plus index indirect; base plus index push/pop; base push/pop; program counter plus displacement; program counter plus displacement indirect; indexed; direct register operand; and immediate operand
Registers:	18
Interrupt Levels:	64 (vectored), allowing interrupts to be set at the channel level
Options:	Watchdog Timer; Full Control Panel (6/34); Basic Control Panel (6/36, 5-slot version)
Memory	Provides up to 64K words of storage in 8K modules
Type:	4K N-MOS
Cycle Time:	650 nanoseconds
Options:	Memory Save and Autorestart; EDAC (Error Detection and Correction), for Model 6/36
Multiple Device Controller	Controls up to four devices using Device-Pacs (i.e., adapters)
Type:	Four levels of simultaneity
Throughput:	32,500 words per second
Mass Storage Controller	Controls up to four disk units, with total capacity from 2.5 million to 40 million bytes.
Type:	One data transfer operation concurrent with multiple seek operations
Throughput:	312,500 bytes per second

TABLE 1-1 (cont). SUMMARY OF LEVEL 6 COMPONENTS

General-Purpose DMA Interface	Provides user interface point for attachment of user-designed adapters
Type:	Single level of simultaneity
Throughput:	400,000 words per second (memory to user device); 500,000 words per second (user device to memory)
Multiline Communications Processor	Controls up to eight full duplex lines at speeds ranging up to 72,000 bps
Type:	Programmable
Interfaces:	EIA RS232C, MIL 188C, Broadband CCITT V35, direct connect, Bell 301/303
Throughput:	Up to 160,000 bits per second

Software (see Figure 7-1 for a complete list)
   Executive Modules
   Program Development Tools
   Input/Output Modules
   Programming Languages (Assembler, FORTRAN)
   Utility Programs
   Loaders and Simulators

Peripherals
   Teleprinters (ASR33/KSR33)
   CRT Display (12 X 80 lines)
   Keyboard Typewriter Console (30 characters per second)
   Diskettes (401,016 bytes/disk, unformatted)
   Serial Printers (60 lines per minute, 132 characters per line)
   Line Printers (240, 300, 480, 600 lpm, 136 characters per line)
   Card Readers (300, 500 cards per minute, punched and mark-sense)
   Cartridge Disk (up to 40 million bytes per controller)

Model 6/36 (Figures 1-1 and 1-2) includes a central processor mounted in a five-slot or ten-slot Megabus chassis expandable to 23 slots; a full control panel; multiply/divide hardware; a real-time clock; and the ROM bootstrap loader. Options include a memory controller with either parity or EDAC[1] memory; 8192-word Memory-Pacs providing a maximum of 65,536 words, and all the options available with Model 6/34. The central processor requires one circuit board; maximum memory requires two boards. Up to 20 additional boards can be attached, for controllers of peripheral devices and/or communication lines. The Level 6 power supply and air circulating unit are included in the assembly housing the central

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[1]Error Detection and Correction.

processor. All software and peripherals listed in Table 1-1 are available with Model 6/36.

The physical configurability of these models is extremely flexible, reflecting the variety of uses to which Level 6 can be put. The overriding consideration has been to provide a low-cost, modular, building-block system with minimal space and power requirements. Functional elements plug into or attach to each other without difficulty, needing little time and skill for assembly, disassembly, and replacement. These characteristics make Level 6 attractive to:

1. Original equipment manufacturers, who demand a minicomputer easily embedded in their own systems, operable and durable in a wide range of environments, and including the ready availability of spare parts and simple repair procedures.

2. Users who will place a Level 6 central processor in their own racks or attach it as a freestanding module, as a tool for various technical tasks (e.g., to collect, communicate, control, or manipulate data in factory and laboratory environments).

In addition, the peripherals available with Level 6, along with the program development and other software, make Level 6 attractive to:

1. Users requiring a relatively complete system, including I/O equipment, for dedicated applications in factory and other non-office environments.

2. Users requiring turnkey systems in various hardware configurations for use in an office environment.

3. Users requiring a program development capability supporting the above applications and generally used in an office environment.

The packaging of the Level 6 models has been designed to satisfy all of these requirements. There are drawer units 5¼ and 10½ inches high for standard EIA rack mounting. There are 60-inch-high cabinets for central processor, diskette, and other drawers. There are tabletop configurations, completely enclosed, completely portable. All provide easy front access and require only front-to-rear airflow for cooling. (In many other minicomputer systems, large backboard areas force designers to use side-to-side cooling with the attendant difficulties of avoiding recirculation in cabinet configurations.)
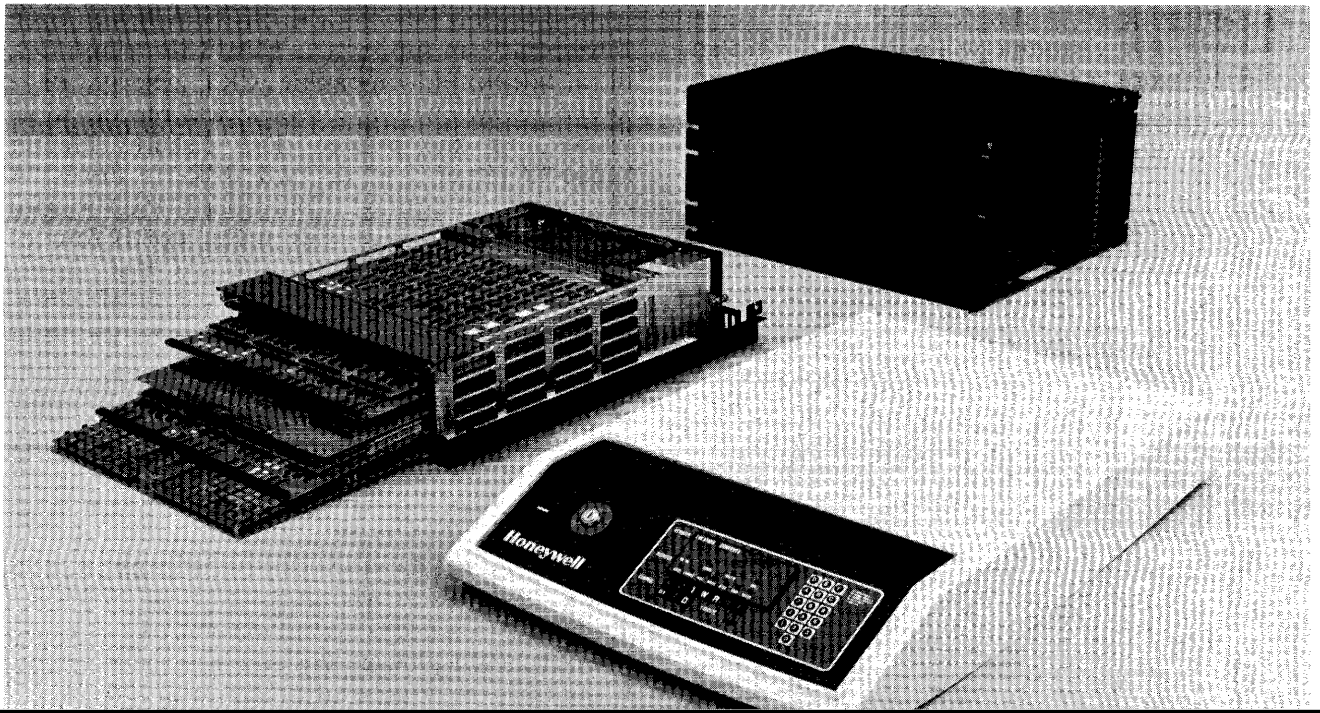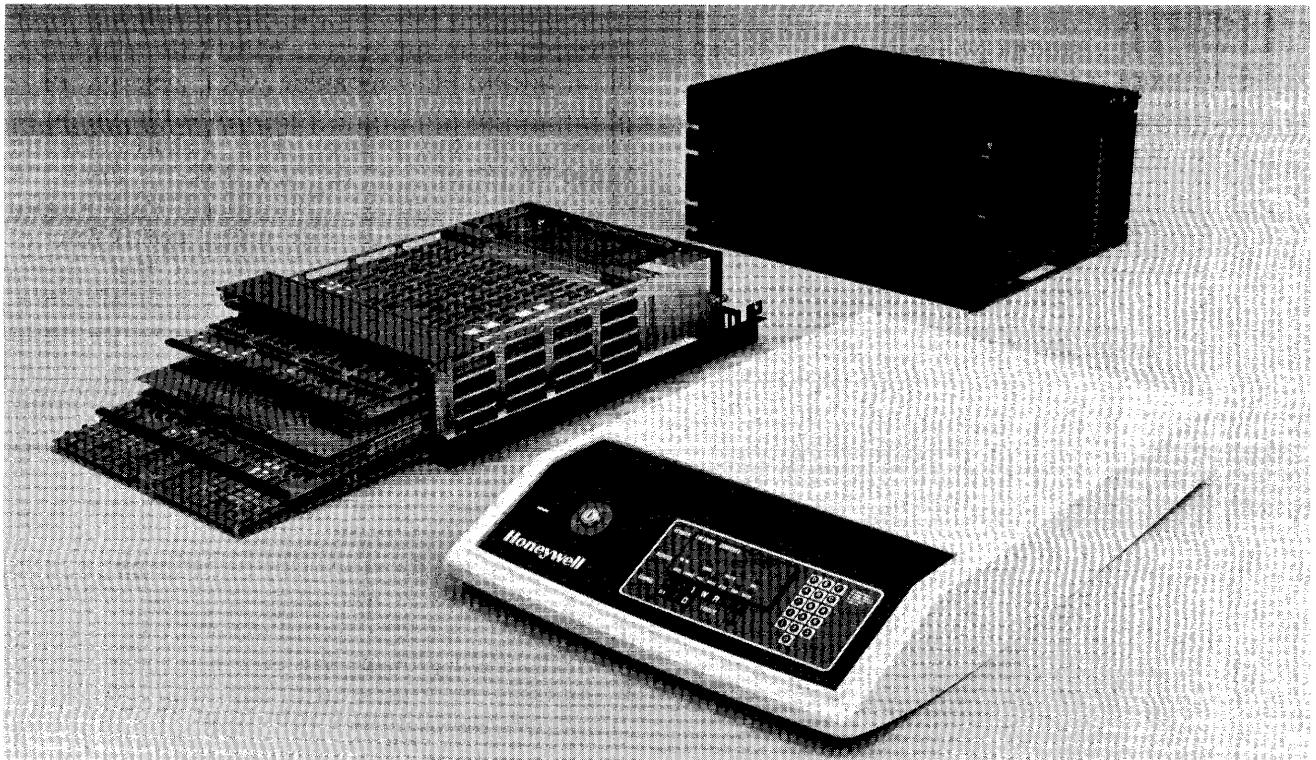
Figure 1-1. Model 6/36 Tabletop Unit and Chassis

Figure 1-2. Typical Model 6/36 Configuration

The software set is also designed to help keep costs down. Every module will operate within the basic 8192-word memory of both models, except for the FORTRAN compiler, which requires 16,384 words. Program development requires only the addition of a teleprinter (or keyboard typewriter console) and a dual diskette.

BOARD TECHNOLOGY

Level 6 uses a primary circuit board 15 inches wide by 16 inches deep (see Figure 1-3). The rear of the board is connected to the Megabus, while devices are connected to the front of the board. (Figure 1-4 illustrates the extreme simplicity of Level 6 connections.) Both Small Scale Integration and Medium Scale Integration are used.

Each memory board can contain up to 32,768 words of memory in four modules (called Memory-Pacs), of 8192 words each. Each Memory-Pac is implemented as a small board, 6½ inches wide by 6½ inches deep, plugged directly into the primary board.

A similar arrangement is used for device and communication controllers (see Figure 1-5). The Multiple Device Controller (MDC) consists of a primary board (containing a microprocessor) onto which up to four device adapter boards (3½ by 11

inches), called Device-Pacs, can be plugged. Each Device-Pac can support an ASR/KSR teleprinter, or a teleprinter-compatible CRT display, or a keyboard typewriter console, card reader, serial printer, or line printer. The diskette adapter supports either one or two diskette drives. A separate Mass Storage Controller (MSC) is used for Level 6 cartridge disk units, up to four of which can be attached to a single MSC. In its control concepts and interface with the Megabus, this controller is similar to the MDC.[1]

The Multiline Communications Processor (MLCP) consists of a primary board (also containing a microprocessor) with up to four line adapter boards, called Communication-Pacs. Each Communication-Pac handles one or two full-duplex lines.

The General-Purpose Direct Memory Access Interface, for users who wish to attach their own devices to Level 6, is also implemented as a single primary board plugged directly into the Megabus. It contains both a Level 6 interface and a large "unpopulated" area for the user's own design interface. (A documentation package included with the interface provides design procedures.) Besides simplifying the connection of user

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[1]See Section 6 for a description of all peripheral devices.
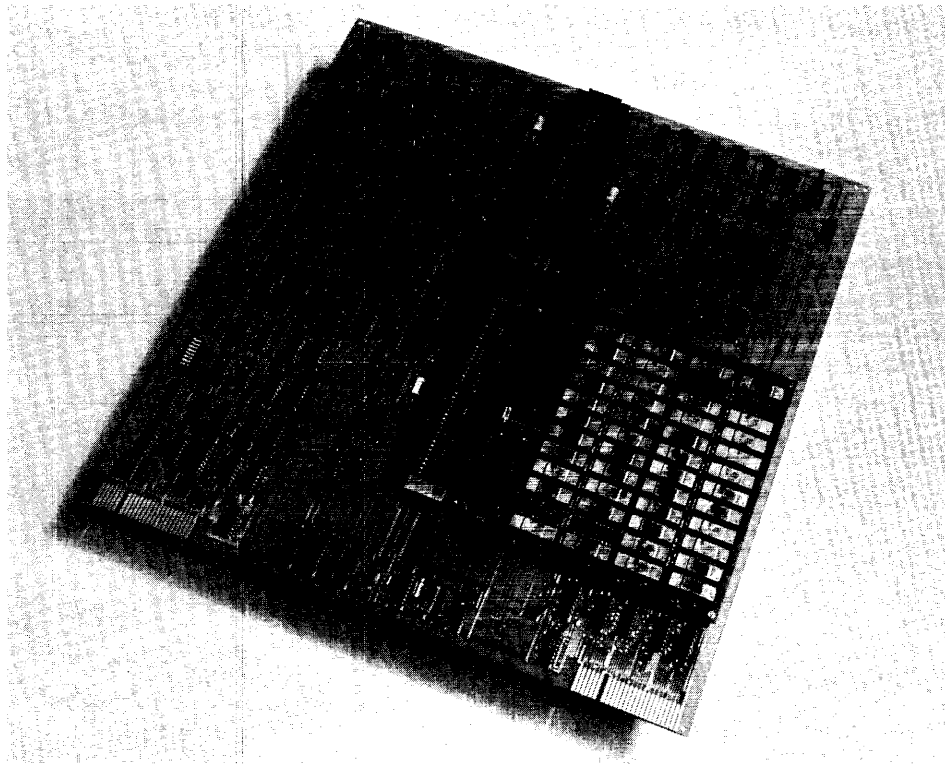
Figure 1-3. Level 6 Circuit Board (Memory Controller with 8 KW Memory-Pac)
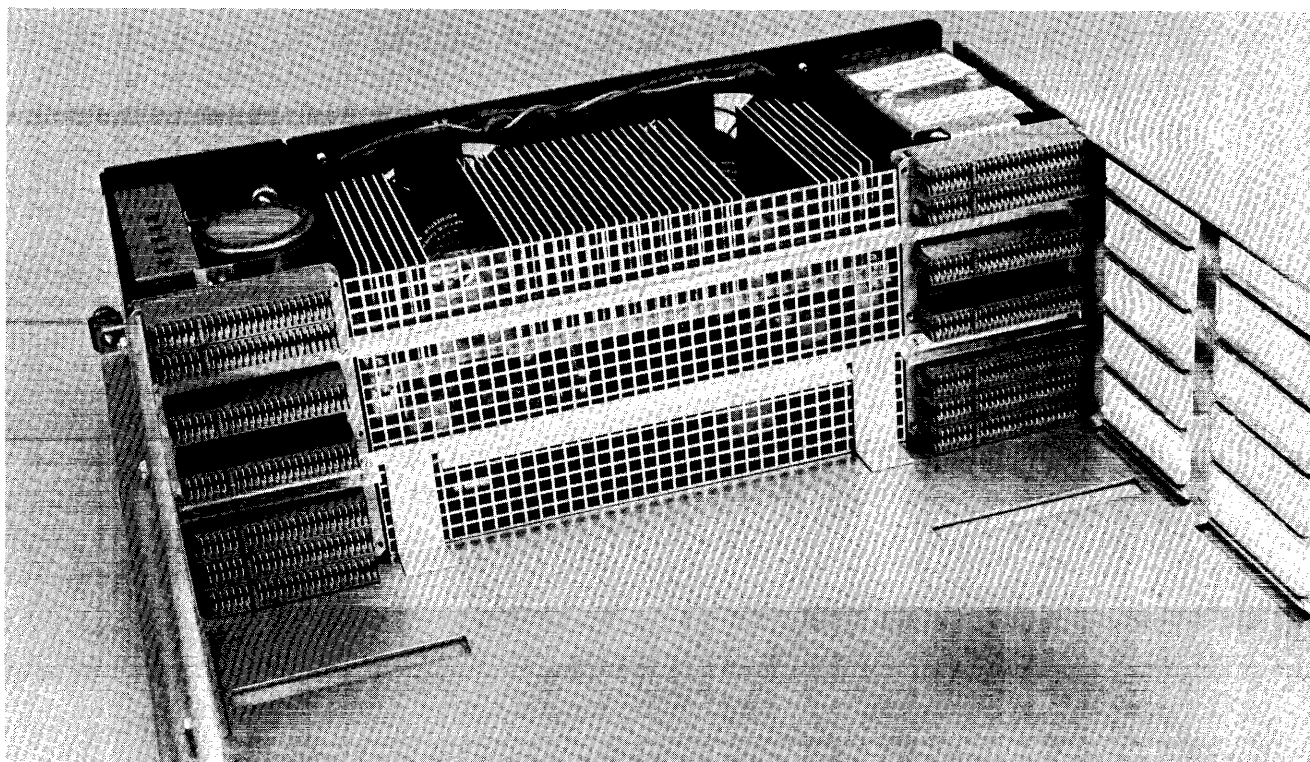
Figure 1-4. Level 6 Megabus and Power Supply

devices, the interface protects the rest of the system from a failure of one of these devices.

Each Level 6 primary board is individually replaceable without disturbance of any other board. Each board and Pac provide so much functionality that Level 6 is physically more compact than most of its competitors. Furthermore, the use of the primary board/Pac concept permits the sharing of costly logic (memory error correction, controller microprocessors) among an unusually high number of basic elements (memory, devices) with very flexible configurability. Thus the Level 6 approach satisfies users' demands for economy in four critical areas: space, power, cabling, configurability.

In addition, board addresses are easy to configure. There are 2^{10} possible addresses. Users can configure an address by setting a hexadecimal rotary switch (establishing an address for each board). This feature is important to all users, and especially to system builders planning to develop software on a large configuration and then use it on many smaller, differently configured systems. Level 6 also includes a device-identification feature; this is independent of software, so users will not have to keep changing their software when they change an address.

Note also that the microprocessors make these controllers more capable, relieving the central processor of many tasks, and also enhance their diagnostic capability.

SYSTEM ELEMENTS

Megabus

The Megabus is the heart of Level 6, central to its performance. All elements of Level 6 — central processor, memory, and device and communication controllers — are attached to the Megabus and all transfers (memory, interrupts, instructions) between them take place on the Megabus. Communication among these elements is asynchronous, permitting elements of different speeds to operate efficiently.

With up to 1024 I/O addresses available, very large I/O configurations are possible (see Figure 1-6). In addition, the Megabus offers an unusually high transfer rate: 6 million bytes (i.e., halfwords) per second (300 nanoseconds per 16-bit transfer cycle).

The Megabus is based on TTL technology. Etched wires are used to join connectors, which means that fewer connections are required, user costs are lower, and bus operation is highly
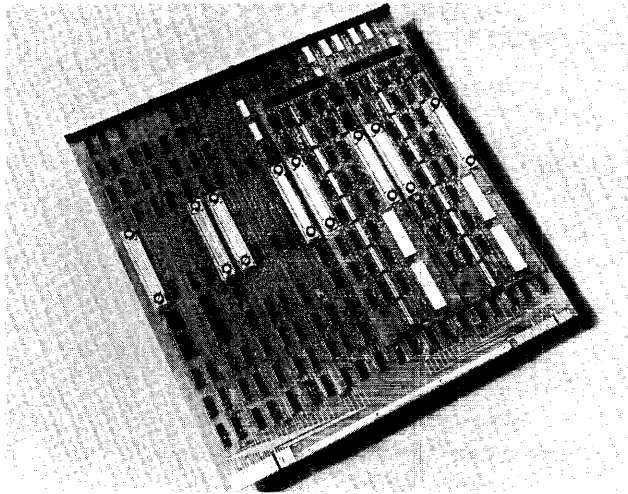
a. Multiline Communications Processor
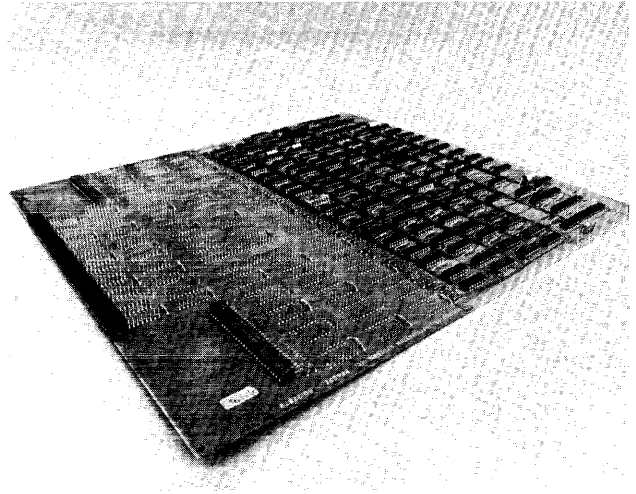
b. General-Purpose DMA Interface
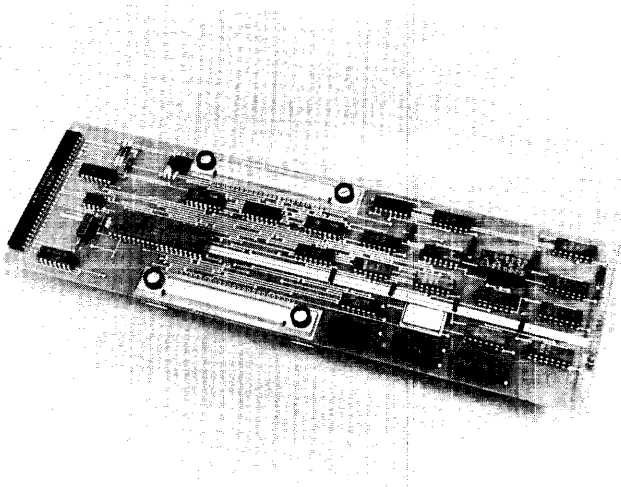
c. Teleprinter Device-Pac
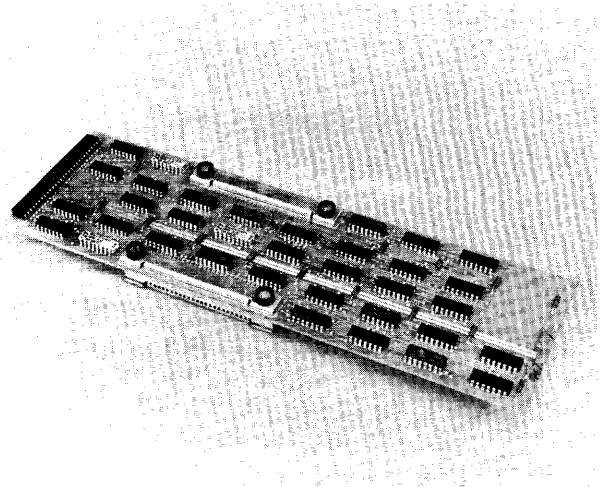
d. Card Reader Device-Pac

Figure 1-5. Typical Controller Boards and Device-Pacs
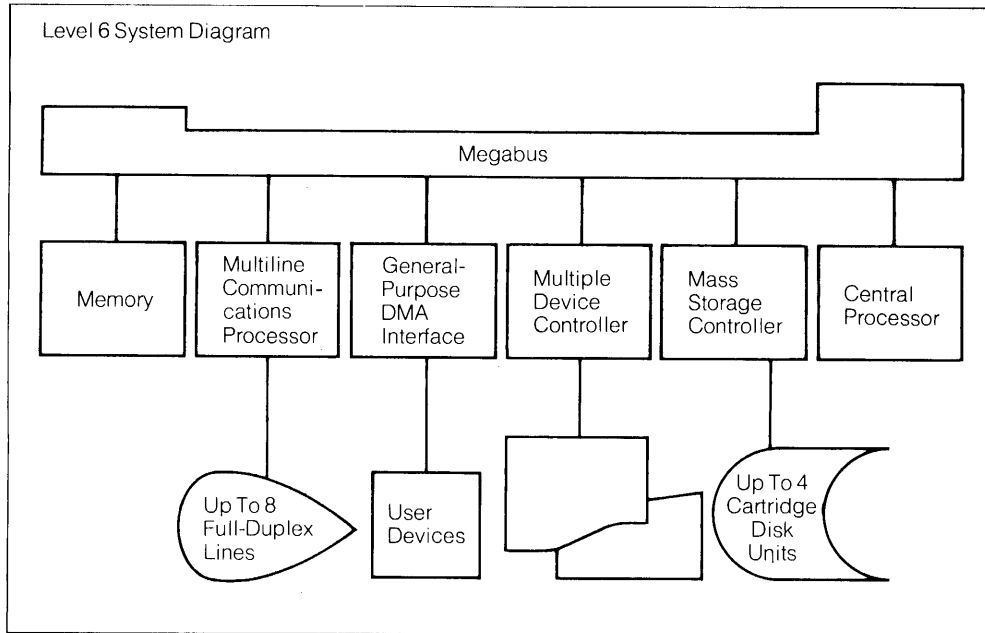
Figure 1-6. Megabus Configuration

reliable. There are 64 vectored-interrupt levels, with 64 priority levels. There is automatic interrupt identification, as when a device interrupts and identifies itself to the central processor. There are no private wires for interrupts; an interrupt is handled as just one of several types of message transmitted on the bus. The Megabus also has an automatic save/restore of context (done on other systems by software): more context is saved in a given time than on competing systems. Parity checking on the Megabus ensures the integrity of data transfers.

The Megabus can transfer either words or bytes. Memory is used efficiently, and controller transfers can start or end on arbitrary byte boundaries. All transfers are of the DMA (Direct Memory Access) type; each device controller maintains its own information about the location in memory to/from which data is to be transferred and accesses that location directly. DMA means that software involvement is minimal. As a corollary, there is distributed Megabus control. Each unit on the Megabus contains all the control and timing it needs to use the bus, without dependence on a central control unit of any kind. This contributes to the great configurability of Level 6.

A distributed tiebreaking network provides the function of granting Megabus cycles and resolving simultaneous requests. The logic to accomplish this function resides in every unit on the Megabus. Priority is granted on the basis of physical position. In any Level 6 system, memory is granted highest priority and the central processor the lowest. Other units are positioned by each user on the basis of their performance requirements, their priority increasing according to their proximity to memory.

To prevent Megabus hangups, including an address to a nonexistent unit, there is a dead-man timeout by the central processor. It times all Megabus transfers and initiates a trap if a slave does not respond within 5 microseconds.

For an overview of system logic and a more detailed account of Megabus interaction with other system elements, see Section 2.

Central Processor

The Level 6 central processor, using TTL technology, is a state-of-the art device, open-ended, powerful, and flexible. The word size is 16 bits — which makes the most of combined economy and functionality. Key features of the architecture may be summarized as follows:

- 18 program-visible general registers, including multiple accumulators and multiple address, index, and control registers and a program counter
- Bit, byte, and word instructions
- Bit test, set, and mask capability
- Immediate, register-to-register, and register-to-memory operations
- 64 vectored interrupt levels
- Multiple vectored trap structure
- Hardware-supported context save and restore
- Multiple addressing modes, including indexing, indirect addressing, base plus displacement, program-counter-relative, auto increment/decrement, etc.
- Permanent bootstrap
- Power failure detection
- Real time clock and watchdog timer (50/60 Hz)
- Automatic restart
- High configurability

These features are described in detail in Sections 3 and 4. In additon, the central processor control panel is described in Section 5.

The instruction set is programmer-oriented, facilitating the writing of compact, efficient programs and offering the right instruction for each function. The multiple word length capability makes it easy to handle data elements of varying size, while the indexing techniques, completely integrated into the architecture, are superior to any competitive system.

The instruction set design strikes a highly effective compromise between two groups of conflicting user requirements: on the one hand the desire for more and more operation codes, more and more operands, more and more flexible ways of addressing an operand; on the other hand, the reluctance to devote extra space in costly memory to longer and more exotic instructions, many of which are infrequently used.

The Level 6 approach defines a 16-bit instruction format that is extended in a number of ways. For example, a 16-bit instruction does not contain a direct memory address (though it does allow the programmer to address memory). For a direct address, a field is added to the instruction; this may be a 16-bit direct address. Thus a 32-bit instruction is achieved as needed. Another method is to use a 16-bit displacement relative to the program counter. The result of this approach is to realize added power only when it is required — without compromising the design of the 16-bit instruction in which most of each program is actually written.

A bootload capability is included on the CP board. It is a ROM stored process and therefore

permanent. There is no elaborate load procedure or multiple keying. Users can select any device through the control panel and bootload from there, providing only the device address (if the bootload is not from the default bootload device). Other outstanding characteristics of the central processor are as follows:

The maximum Level 6 memory (131, 072 bytes) can be *addressed directly* (i.e., without an "indirect address" elsewhere in memory); the complexities and overhead of paging/segmentation units are avoided.

The Level 6 indexing technique permits *addressing and manipulating bits and bytes* in memory. Bit instructions allow testing, setting, resetting, complementing, etc. addressed bits. Byte instructions allow logical and arithmetic operations. Both facilitate the writing of compact, efficient programs.

The 18 *programmable registers* include 7 address registers, 7 data registers, 3 index registers (using data registers), 3 control registers, and a program counter. This is a large complement for a minicomputer. Programs can be more compact and execution times faster than on machines with fewer registers.

The Level 6 *interrupt structure,* with its associated firmware-level dispatching and automatic context save/restore (see above and also "Executive Modules" in Section 7), efficiently maintains a 64-level priority system while eliminating the need for complex software to perform this function.

Hardware trap support of up to 20 trap conditions allows quick handling of exceptional conditions (e.g., overflow) and permits a source program to run even if a facility it requires is not installed. See "Trap Manager" under "Executive Modules" in Section 7.

Level 6 includes instructions that facilitate *stack and queue manipulation,* including subroutine calls, re-entrant and recursive programming, and data buffer management.

Memory

Level 6 memory offers the reliability, low cost, and high density of MOS components. Battery back-up in the event of power failure is also available as an option (Memory Save and Autorestart).

Level 6 memory is a state-of-the-art semiconductor type using N-channel 4096-bit dynamic RAMs as the storage media. Its design emphasizes high reliability, low cost, modularity, and simplified field maintenance. Like other elements of Level 6 the memory is a Megabus-compatible subsystem which may communicate directly with and in the same fashion as any other element on the bus. TTL MSI circuitry is used liberally to minimize power and space requirements for the extensive functionality provided. Self-contained on each memory module is Megabus support, refresh, and initialization logic.

Byte-parity memory, offered on Model 6/34 and Model 6/36, includes logic for storing/retrieving two parity bits per word on each 8192-word board module. Thus the actual word size in memory is 18 bits. The parity bits are returned to anyone reading the memory.

EDAC (Error Detection and Correction) memory, offered on Model 6/36, includes logic for six parity bits per word on each 8192-word module. The supplied parity is used together with the data to develop and store an EDAC code. When it is read, memory attempts to correct any internally caused data error, reporting the results over two dedicated leads on the Megabus. Each lead sets a specific status bit depending on whether the error can be corrected or not. EDAC is particularly desirable for large systems, where extended reliability is required.

With either kind of memory, address parity accompanies the most significant eight bits on the address bus. When memory detects an error on these bits, it does not respond; the result is a bus timeout. Note also that each device/communication controller on the Megabus checks parity as it passes through and indicates an error by setting a parity error status bit.

Memory Save and Autorestart guarantees data retention for 131,072 bytes of memory for a two-hour period. Support circuit power runs are separated to minimize standby power drain. Electronics within the optional unit maintain battery charge, regulate outputs, and indicate holdup failures.

Semiconductor Storage

Commercially available 4KN MOS devices are used as the storage elements. Each device is exposed to vigorous functional testing on computerized test equipment before undergoing a 16-hour stress cycle at temperature. The result is a cost-effective quality product comparing favorably with core technology in all respects. TTL compatibility offered by N-channel MOS eliminates the need for and liability of the extensive discrete and linear IC circuitry required to interface with core memories. The packing density is superior and power requirements are dramatically reduced: both characteristics again enhance the Level 6 size, weight, and MBTF advantages over core. Furthermore, a straightforward integrated

circuit approach simplifies failure diagnosis and repair procedures as compared with core technology. One other significant advantage over core is the increase in memory utilization made possible with the inherently shorter cycle times associated with semiconductor devices.

Packaging

The advantages of Level 6 board technology are significant. Field expansion in small capacity increments is now possible without the cost of repeating overhead circuitry. Sparing costs are minimized through the use of the 8192-word modules as ORUs.[1]

Functionality

As in the case of other Level 6 system elements, the memory functions with minimum Megabus utilization. The interface is totally asynchronous, and after a memory read request is acknowledged the bus is released to other users. Meanwhile the memory completes its internal cycle while retaining the identification of the requestor. As the internal cycle nears completion, the memory requests a Megabus cycle and upon acknowledgment of bus availability sends data to the requestor. Megabus usage is less than half the memory cycle time and so allows simultaneous utilization of two modules at their maximum cycle rates.

Level 6 addressability extends to 16 million bytes: hence future expansion of the maximum memory now available on Level 6 is foreseeable. Configuration switches mounted on the memory are set with the module identification address to establish each module's position with the address spectrum. (The module's logical position, i.e., address, has no relationship to its physical chassis position.)

Write operations require only one Megabus cycle. Both full and byte write modes are available. Byte writes require a longer internal cycle for EDAC versions,[1] since check bits are now a function of both new and stored data. In EDAC parity checking, "Red" and "Yellow" bus signals are activated for noncorrectable and correctable errors, respectively. Parity on new data is treated as a pseudo data bit by the check bit encoders. If bad parity is received, the "Red" line is activated during the subsequent readout.

A unique maintenance aid, the EDAC bypass feature, is provided on EDAC memories to permit full field verification of the integrity of the error

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[1]Optimum Replacement Units. See below under "Maintenance" for an explanation of the ORU.

[2]Read operations are also somewhat longer with EDAC versions of memory.

correction circuitry. In addition to the EDAC bypass feature, a momentary contact switch is placed on the memory board within easy access behind the swing-out control panel. When the switch is depressed during the specified portion of the diagnostic routine, check bits are forced to all zeros for all new data. With careful selection of data patterns, all elements of the decoding, detection, and correcting logic can be exercised and must be operating properly for the scrambled readout data to match that of a functioning system. Other portions of the EDAC circuitry, including check bit chips, can be checked with special patterns in normal mode.

The sharing of the I/O bus with memory in Level 6 is a departure from much standard minicomputer practice, in which a second bus is dedicated to memory. Advantages of the Level 6 approach are as follows:

1. A fully asynchronous memory interface is achieved that is fully compatible with all other elements of Level 6. Thus direct memory access is a fundamental ingredient of the architecture. Furthermore, the standard asynchronous interface expands configuration dimensionality by allowing simultaneous use of memory types with varying performance and cost.
2. Bus hardware is minimized, with less than 100 signal paths required for the total function. This feature helps make possible the unique physical configuration of Level 6, providing front access board removal in conjunction with the simplicity of front-to-rear cooling airflow.

Multiple Device Controller (MDC)

Each MDC supports up to four of the following devices, via individual Device-Pacs as described above: (1) a standard Model 33 ASR/KSR teleprinter; (2) a teleprinter-compatible CRT display for console use; (3) a 30-character-per-second keyboard typewriter console; (4) a 300 or 500 card-per-minute (CPM) card reader; (5) a 60 line-per-minute (LPM) serial printer; (6) a 240-600 LPM line printer. The MDC also supports one or two diskette units. Through the MDC, all these devices can operate simultaneously.

Multiple MDCs can be attached to the Megabus, and multiple like devices can be attached to any MDC. Each MDC contains a firmware-driven microprocessor augmented with the circuitry necessary to support the adapter connections. All hardware unique to a specific kind of device is contained in the Device-Pac (which makes it easy for users to change their peripheral configura-

tions). Through its Pac each attached device presents a DMA (Direct Memory Access) interface to the central processor. The design of this interface is such that software commands and status pertain to the device itself rather than to the MDC.

A portion of the MDC firmware is reserved for a hardware verification routine called Basic Logic Test (BLT), which supplies a go/no-go visual identification of an MDC hardware failure. Its purpose is to verify basic data paths in anticipation of running ORU isolation and test routines. If the BLT detects an error, that error is isolated to the MDC, which is the ORU.

The Basic Logic Test is invoked in the MDC in response to a Master Clear on the Megabus or an initialize command (issued by software) received on any MDC channel. Results of the BLT appear as a visual indication on the control panel edge of the MDC board and on the control panel itself. An indicator turns on during execution of the BLT and turns off only if the BLT is successfully completed.

Software isolation test routines are provided to verify all operational aspects of the MDC and to isolate failures to an ORU. The operator interfaces with these routines via the CP control panel or a console device. The routines run as stand-alone modules, but Level 6 includes diagnostic functionality to support them.

Mass Storage Controller (MSC)

The Mass Storage Controller provides micro-programmed support of up to four disk units with a total capacity of 40 million bytes. General control functions include execution of Megabus sequences, command decoding, data transfer multiplexing between Disk-Pacs, and status and control register storage.

The hardware unique to the disk units is localized on a Cartridge Disk-Pac similar in concept and performance to the Device-Pacs plugged into the MDC. The Disk-Pac performs such functions as device interface dialog control, sync word detection, check word generation/verification, device state monitoring, and bit-to-bit conversion for the set of disk units (1 to 4) attached to the MSC.

Maximum throughput across the MSC/Pac interface is 312,500 bytes per second. Multiple MSCs can be attached to the Megabus. The MSC permits a data transfer operation to take place concurrently with multiple seek operations.
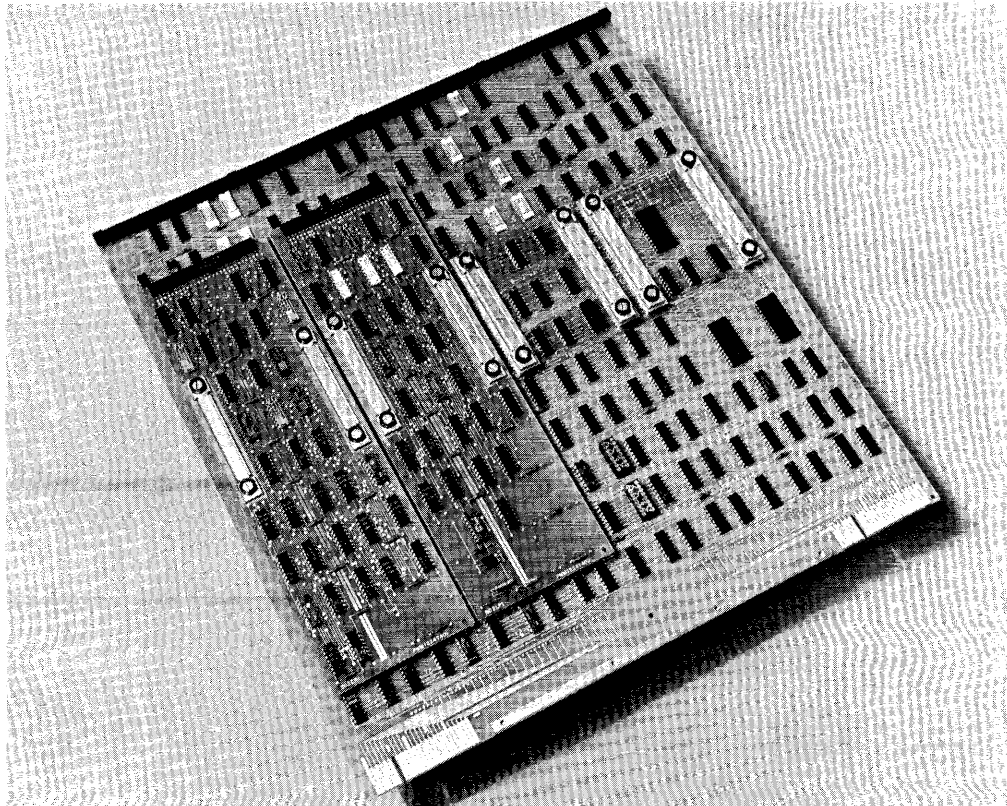
Figure 1-7. MDC with Device-Pacs Attached

Multiline Communications Processor (MLCP)

The microprocessor-based MLCP provides an extremely powerful communications link at moderate cost. Each MLCP can contain up to four Communication-Pacs, and each Pac can handle one or two lines. Throughput is up to 160,000 bits per second. The MLCP is unusually flexible regarding line types, speeds, communications disciplines, etc. For example, it can handle up to eight full-duplex lines in one board slot at speeds to 9,600 bits per second, or it can drive one line at 72,000 bits per second. Its 4096 bytes of Random Access Memory (RAM) — 3072 used for its procedure code — permit it to execute complex line-handling procedures with no involvement of the central processor. Key attributes of the MLCP are as follows:

- Implementation of MLCP on a single primary board with field-configurable, easily changed/replaced Communication-Pacs
- Operation of up to eight full-duplex, 9,000-bits-per-second lines or one 72,000-bit line per MLCP
- Program load of configuration and control
- Program load of data stream control

- User-programmable to provide for message delimiting, message editing, checking algorithms
- Hardware checking (e.g., Longitudinal Redundancy Check — LRC)
- Individual DMA for transmission direction of each line
- Standard Megabus interface and five standard communication interfaces:

> *Synchronous Line Communication-Pacs:* one or two full-duplex lines; speeds of up to 10,800 bits per second; EIA RS232C interface.
> *Asynchronous Line Communication-Pacs:* one or two full-duplex lines; speeds of up to 9,600 bits per second; EIA RS232C interface, one or two stop bits; selection of speeds by parameter.
> *Broadband Line Communication-Pac:* one full-duplex line; speeds of up to 72,000 bits per second; broadband CCITT V35 interface.

Each line direction is considered a channel for which the software can set interrupt levels dy-
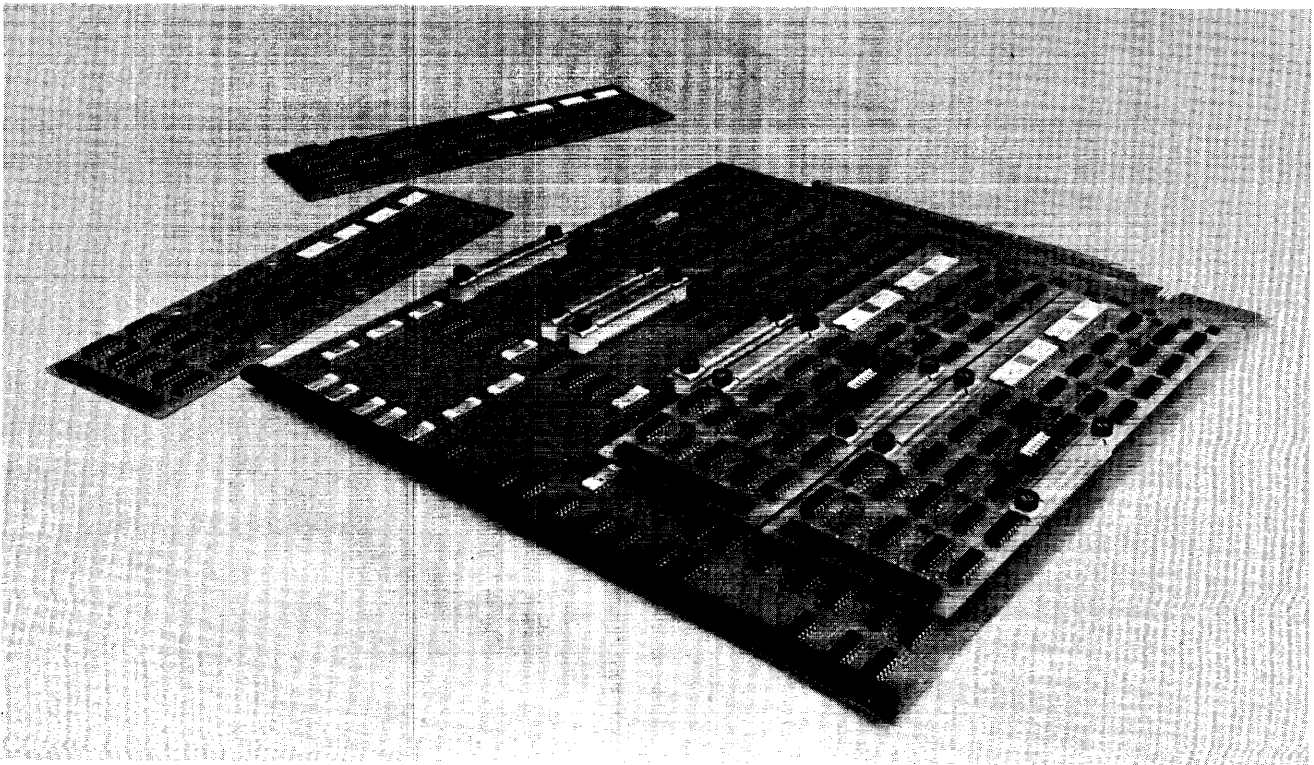
Figure 1-8. MLCP with Communication-Pacs Attached

namically. Modem interfaces conform to EIA RS232C, MIL 188C, and foreign CCITT specifications.

As indicated above, the MLCP microprocessor is programmable at the channel level. These programs can edit and convert prespecified sequences of data. The microprocessor fully delimits the data stream, offloading the central processor of character generation, detection, and block check functions. Data formats, code lengths, and parity characteristics are program selectable for a given line.

The differences between line protocols and the specific requirements of each line adapter/line combination are handled via small software routines residing within the MLCP on a per-line basis. These routines are loaded from an image in main memory by the system operating software and can be re-entrant and shared within the MLCP. With this system, it is possible to reconfigure lines from one protocol to another by simply changing a parameter or reloading a line-specific routine.

Like the MDC, the MLCP uses a Basic Logic Test to verify that the Megabus and the command interface to the MLCP functions are operable to a level at which the ORU Isolation Test Routine can be executed. This BLT is initiated either by hardware (the Master Clear Button) or by software (Initialize Command to the Controller), and the go/no-go results are displayed by an indicator on the MLCP and the control panel. In addition, each of the eight lines has program-usable loop-back of data transmit to data receive to facilitate diagnosis.

General-Purpose Direct Memory Access (DMA) Interface

This interface, implemented on a single primary board (more than one can be attached to the Megabus), provides users with a means of interfacing special devices to Level 6. Its features are as follows:

- word-wide interface
- asynchronous interface
- DMA mode
- ability to interrupt the central processor
- support of multiple devices
- simple control-line interface
- spare area for user logic
- documentation package including design procedures for specific power and isolation requirements

The Interface provides all the circuitry, storage, and control logic required to maintain functionality with the Megabus so that users can easily interface their own controllers to Level 6. It operates in DMA mode, supporting a single channel that can be used in either direction. Data to/from the user is transferred in 16-bit parallel form, controlled by a simple, asynchronous handshake operation. Data transfers between the interface and the Megabus are also in 16-bit parallel form, via DMA control.[1]

A scratchpad memory (16 bit x 16 word) is integral to the Interface. One cell (16-bit word) is dedicated as a temporary data buffer to isolate the user from the bus. Other cells are used for essential system quantities (e.g., Status, Task Word, Interrupt Control). Nine cells are provided for user application as working registers or as communication locations between the user-written driver and the user's hardware.

Board maintainability is enhanced by the inclusion of loop-back logic. This feature, along with the standard test and verification program supplied, allows a user to exercise data transfers under DMA control, as well as scratchpad memory operation and task flag and interrupt functions.

The Interface board contains both the Honeywell-supplied logic and an area reserved for user logic (see Figure 1-9). The user area is configured with 66 sites for mounting 14- or 16-pin Dual in-Line Packages (DIPs). Each DIP station includes wirewrap pins for the user interconnections. The interface logic and user areas are separated by a row of 70 wirewrap pins; of these, 50 are used to connect the interface signals to/from the Interface logic (the rest are used for power and ground). There are two 56-pin connectors for attaching cables to user devices.

POWER SUPPLY AND AIR CIRCULATING FANS

The Level 6 50/60 Hz power supply and air-circulating fans are located at the rear of the drawer holding the central processor. Packed into a relatively small volume (about 15 inches wide by 6 inches deep by 5 inches high) and requiring only a standard, 120-volt, single-phase, 3-wire supply, the power module provides users with unusually economical operation plus full brownout protection (it can ride through a 3- to 4-cycle loss).

The front panel and chassis wraparound provide complete protection from hazardous voltages. In addition, the ac line input is interlocked so that removal of the power supply automatically removes ac power from the system.

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[1]Transfer rates: 0.4 million bytes/sec from memory to user device; 0.5 million bytes/sec from user device to memory.
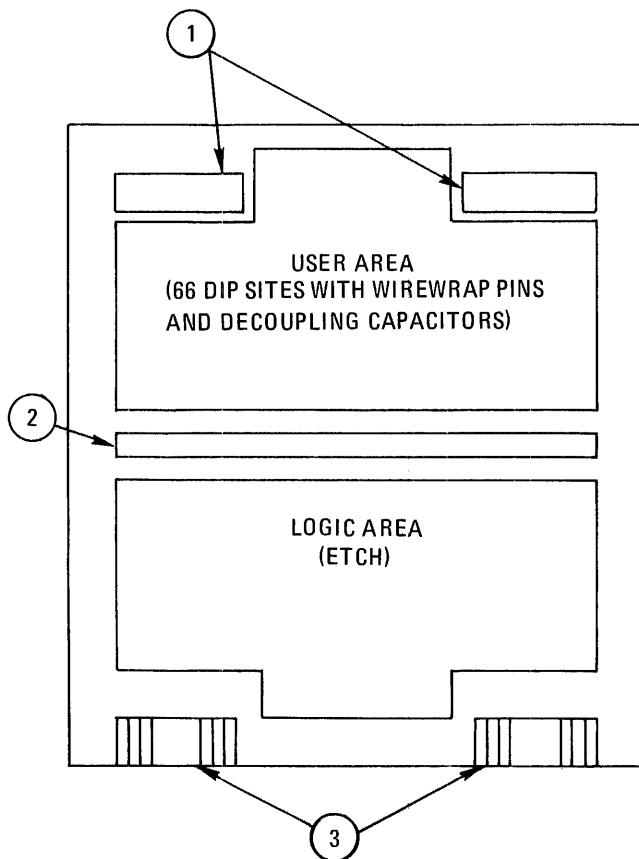
① Two 56-pin connector receptacles for user application; include mating edge connectors.

② Row of 70 staked pins (wirewrap) providing interface signals for user interconnection.

③ Edge connectors; plug into Megabus.

Figure 1-9. Layout of General Purpose DMA Interface Board

Two fans mounted at the rear of and as part of the power supply draw air from the front to the back of the drawer, past the circuit boards and the power module itself. They help keep the system operating through a temperature range of 0°C to 50°C ambient, and a humidity range of 5% to 95%. Both power supply and fans have UL approval.

PERIPHERAL DEVICES

Level 6 includes a set of economical peripheral devices, all attachable via the MDC or MSC,' featuring quiet operation suitable for an office-like environment, low power requirements, and sufficient speed for any user application. This section summarizes peripheral features; for detailed information, see Section 6.

Programmable Interrupt Levels

Level 6 gives any peripheral device the capability of interrupting at any level, under software control. Interrupt levels can be set by the software dynamically, before each job or before each peripheral instruction sequence, etc. These levels are independent of physical system configuration or device type. Users benefit from an increased flexibility in assigning job priorities.

Teleprinter and Compatible CRT Device

Teletype Corporation standard Model 33 teleprinters are available in a Level 6 packaging design, in either ASR or KSR versions.

The console display is a low-cost, teleprinter-compatible device for users who require a visual medium in addition to their hard-copy teleprinters and typewriter consoles. It features a separable keyboard (facilitating its use and incorporation into office furniture packages), nondestructive cursor backspace and forwardspace, and a 960-character (12-line) display. A 64-character set (ASCII) is standard; a 95-character set including lower-case letters is optional.

Keyboard Typewriter Console

The keyboard typewriter console prints 30 characters per second and has a line width of 132 print positions. The ASCII character set includes upper- and lower-case letters, 10 numerals, punctuation marks, and special symbols. Paper is tractor-fed and the fanfold paper forms provide lengths of 3 to 17 inches and widths of 4 to 15 inches. The console furnishes an original and four clear copies.

Card Readers

Level 6 card readers handle 80-column cards (or, optionally 51-column cards) at 300 or 500 CPM. A Mark Sense capability allows the reading of mixed punches and IBM-compatible marks. The hopper and stacker capacities are 500 cards. The card readers are packaged for table-top mounting and have UL and CSA[1] approval.

Serial Printer

The serial printer furnishes an original and up to four clear carbon copies at a speed of 165 characters per second (CPS). This speed is equivalent to 60 lines per minute at 132 characters per line.

There are 132 print positions at a horizontal spacing of 10 characters per inch. Characters are formed from a 9 by 7 dot matrix and are equivalent to 10-point type. The printer has a

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[1]Canadian Standards Association.

vertical spacing of six lines per inch and a capability for Head of Form, End of Form, and Single Line formats. There is a standard set of 64 ASCII characters and an optional set of 96 characters. A standard sprocket paper feed is used.

The printer has an eight-bit parallel data interface for connection to the Device-Pac.

Line Printers

The line printers operate at 240-600 LPM, using the standard 64-character ASCII set or optional 96-character ASCII set. Characters are printed from a drum-mounted solid font.

There are 136 print positions, and the paper has a slew rate of 20 inches per second. Six-part forms are produced. A Vertical Format Unit provides Head of Form and End of Form capability in a 66-line format; a 12-channel paper tape option is available for the VFU.

A floor-mounted cabinet is standard. The line printers have both UL and CSA approval.

Diskette

The Level 6 diskette capability is offered as a subsystem including the Device-Pac for the MDC and two diskette devices. These devices appear completely independent to the software, since a command addressed to a channel that is not busy is always accepted. All operations are executed simultaneously on the two units, except for data transfers: in this case the MDC accepts a data transfer command for one device but does not transfer data until an on-going transfer on the other device has been completed.

The subsystem uses standard (IBM "Type 8") flexible magnetic disks or their equivalent. Data is physically recorded on the disks in an IBM-compatible format, but the contents of the header records and the actual data are under software control and are not restricted to be IBM-compatible. The data representation is in ASCII. The software is optionally capable of translating from ASCII to EBCDIC to produce a diskette that may be interchanged with IBM equipment.

The diskette has a data rate of 31,248 bytes per second (MDC to memory) and a capacity of 256,256 bytes per disk (formatted, 77 tracks).

Cartridge Disk

The cartridge disk unit provides low-cost data storage for users with medium-sized file requirements. Each unit has a capacity of 2.5 to 10 million bytes; random access to 10 million bytes requires an average of less than 50 milliseconds.

Record lengths can be varied to suit user applications; all records include check words for data integrity. The units are packaged for either rack or cabinet mounting; both versions feature easy top-loading of removable cartridges. And since removable and fixed disks can be mounted on the same spindle, file copying can be accomplished with a single unit.

SOFTWARE

Level 6 offers both a basic and an extended software capability, in packages called respectively, GCOS/BES1 and GCOS/BES2. Under GCOS/BES1 the chief system functions are performed, allowing users to concentrate on their individual applications. A set of executive modules provides a rapid response to time, priority, and I/O interrupts. Their size is minimal and their interface with user programs is straightforward and easily learned. Providing basic system control and firm base on which to build applications, their features include: task management — starting, suspending, and resuming specific tasks on the basis of software priority levels; support of the central processor real-time clock to provide both periodic and time-of-day execution; operator interface management; trap management; and optionally, dynamic buffer allocation allowing a number of requesting tasks to share memory.

For program development, GCOS/BES1 includes both a powerful 8K Assembler and an industry-standard 16K FORTRAN compiler. Either language operates in a minimum Level 6 configuration with two diskettes but takes advantage of larger Level 6 systems. Compilation and testing are operator controlled via a command processor that uses simple, keyed-in commands to permit all Level 6 operations.

The Assembler uses a free-form language that allows the programmer to take maximum advantage of the Level 6 hardware/firmware instruction set. In two passes, the Assembler produces relocatable code for a program of up to 32K. Programmers/operators can choose to suppress the object file or a listing, list error lines or conditional lines only, or set a conditional switch value. The single-pass FORTRAN compiler provides full Level 1 ANS1 1975 functionality. For greater flexibility, programmers/operators can specify standard relocatable output or Assembly source text. In addition, assembly language statements can be imbedded within a FORTRAN program.

To assist the program development effort, GCOS/BES1 includes a linker that can process

150 external references to build a 64K image file and a productivity-increasing text editor. Still other BES1 software includes loaders that support relocation and accept files from card reader, console paper tape, or diskette; online and standalone device drivers supporting terminals and peripheral devices (programs can be written to incorporate the standalone device drivers or to call the Executive, which will then handle input/output); and a configuration load manager that performs system generation, configuration, and initialization.

GCOS/BES2 includes all the capabilities of GCOS/BES1, with significant extensions in communications, executive functions, and program development tools. Among the new communications capabilities are support of a BSC link to a host computer and an operator interface. Added executive functions include a disk-based system loading/activating tasks resident on either diskette or cartridge disk. And the program development enhancements encompass extensions in both the Assembler and the FORTRAN compiler and macro processor. There are still other capabilities in such areas as file management, utilities, job stream management, and teleprinter/console display support.

For a detailed discussion of GCOS/BES software, see Section 7.

HUMAN FACTORS ENGINEERING AND INDUSTRIAL DESIGN

Level 6 hardware elements meet OSHA[1] requirements for operator safety. They have UL and CSA approval. Safety-interlocked panels help eliminate operator hazards, work surfaces are made of durable materials and finishes, and casters and jacks ease installation.

There are many operator convenience features: "see only when necessary" status displays plus internal illumination to avoid confusion and reading errors; insulation to reduce noise; easy machine loading procedures; high-lubricity feed and stacker work surfaces for efficient document handling; simplified access to card paths to facilitate the removal of damaged cards.

In addition, system builders benefit from the great flexibility of Level 6 in installation and configuration, from the need for less power and floor space than in many competitive systems, from the easy accessibility of internal components and the overall design for simplicity of operation and maintenance, from the greatly

reduced requirements for operator training, and from the feasibility of personalizing the equipment.

SITE PREPARATION PLANNING

Some users need very little site preparation assistance; others need detailed pre-installation planning. As a major mainframe producer Honeywell has had years of experience in installing computer systems and can provide assistance at whatever level is required. Both end users of Level 6 and system builders incorporating Level 6 components into their own product lines will find Honeywell's knowledge and expertise helpful, either in forestalling difficulties or in solving particular configuration problems.

Honeywell's assistance covers the range of physical, environmental, electrical, and safety requirements. Section 8 provides planning information in detail, including configuration, layout, specification, and site facility data.

MAINTENANCE

The Level 6 design concept, based on containing functional system modules on single boards, not only reduces module interconnections to Megabus and power (eliminating intra-module connections) but also enhances system availability: First, the existence of functional boundaries simplifies the procedures required to diagnose faults. In turn this means that execution of these procedures should require very little downtime, on the order of minutes, and that the attempt to isolate a fault to board level should normally be successful. Third, "repair" of the fault requires simply unplugging the failed unit and plugging in a replacement.

For maintenance purposes, all system modules that can be easily removed and replaced at the customer site are called Optimum Replacement Units, or ORUs. Either Honeywell field engineers or user personnel (nontechnical but trained) will replace an ORU, depending on the maintenance agreement in effect. ORUs include the following:

- Primary boards that connect into the Megabus and similar boards that form part of a Level 6 component (e.g., Memory- or Device-Pacs).
- A power supply, control panel, or peripheral device.
- Fuses for power; air circulating fans.

The actual ORU isolation is carried out in two steps. First the resident hardware/firmware performs the go/no-go test of basic data paths to

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[1]Occupational Safety Health Act

verify that ORU Isolation Test Routines are loadable and that their execution can be initiated. Second, these software tests are performed, completing the ORU isolation and causing the results to be displayed.

The display of results indicates (1) the unit to be replaced, (2) the case of no fault detected, or (3) the case in which the fault cannot be resolved to an ORU. In the vast majority of cases the result will be isolation of the fault to an easily replaced ORU.

DOCUMENTATION

Level 6 documentation includes a full, integrated set of software, hardware, and other manuals. These are user-oriented, written for easy operational and reference use. Every major element of Level 6 is documented.

FUTURE DEVELOPMENTS

Experienced minisystem users will have noticed that the open-ended design of Level 6 holds truly exciting possibilities for hardware or software extensions into many areas, with benefits to themselves in terms of greater functionality and bottom-line economies. Your Honeywell Marketing Representative will keep you abreast of these developments. In addition, Honeywell will continue to make largely invisible improvements in Level 6, whose architecture accommodates the rapidly developing semiconductor technologies. Level 6 is built to last: to provide what you need now and in the future, at a definitive cost/performance advantage over its competitors.

SECTION 2

SYSTEM ARCHITECTURE

CONNECTABLE UNITS

There are three principal types of units in all 6/30 systems: central processors, input-output controllers, and memories. One or more of each type can be included in a system. All are interconnected by the Level 6 Megabus.

Up to 23 connectable units are supported by Model 6/36, and up to four by Model 6/34. In this context, a connectable unit generally is synonymous with a board and can be any one of the following:

— a central processor
— a memory controller with 8K-32K 16-bit words of memory
— a multiple device controller (MDC) capable of supporting up to four different devices
— other peripheral controllers

— a multiline communications processor (MLCP) capable of supporting up to 8 full-duplex lines
— a general-purpose direct memory access (DMA) interface (GPI) to which customers can connect their own I/O device.

Several controllers of the same type may be included in a system. Each is identified by a unique module address which is easily field-adjustable. Figure 2-1 shows a 64K Model 6/36 system with 3 MDCs and 1 MLCP. This system could support, for example, 4 diskettes, 2 printers, 4 CRTs, a card reader, a teleprinter, and up to 8 communications lines to remote terminals and/or host processors. Yet only seven connectable units are required, and a 10-1/2 inch, 10-slot 6/36 chassis would have 3 empty slots for future use. If further expansion were required, additional chasses could be added until the 23 module capacity was reached.

A 6/30 system can have up to 64K words of memory. Typically this is housed on two controller boards attached to the Level 6 Megabus. However, in certain cases it may be advantageous to split 32K words of memory between two or more boards, allowing a greater degree of overlap to take place in the system. Figure 2-2 shows two ways of configuring a 48K memory. The standard way is to use two controllers, the
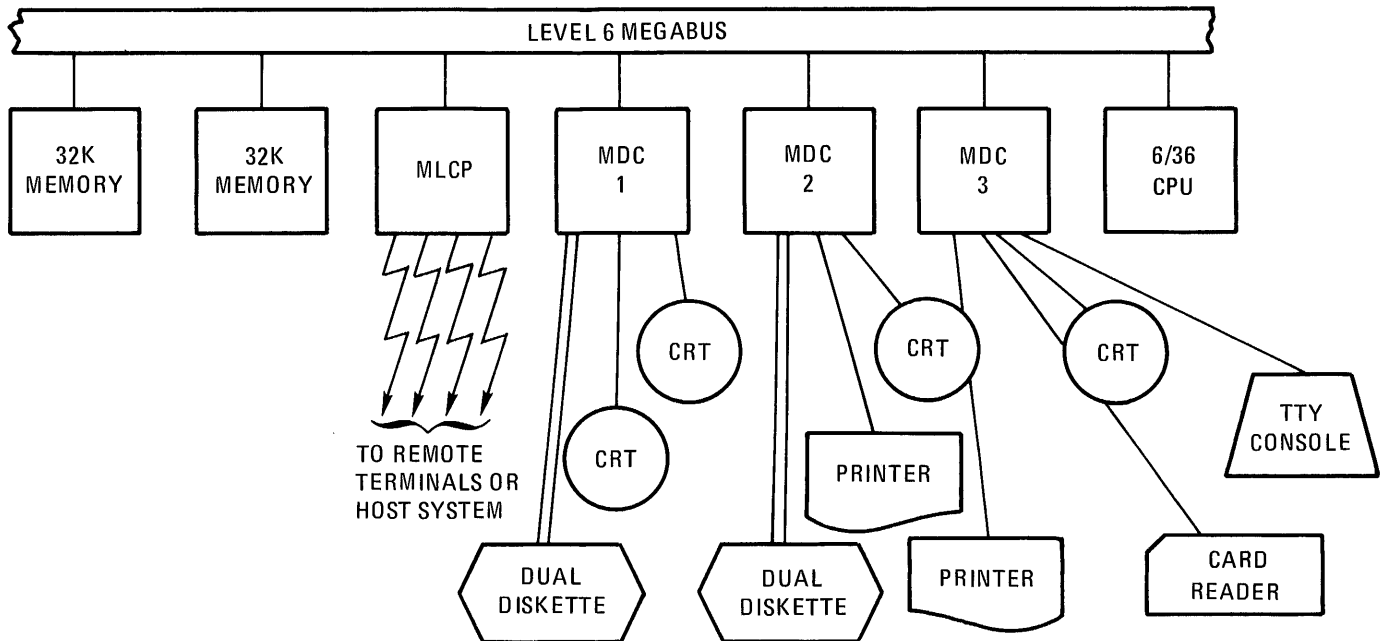
Figure 2-1. Typical 6/36 Configuration Diagram

STANDARD 48K CONFIGURATION

ALTERNATE 48K CONFIGURATION
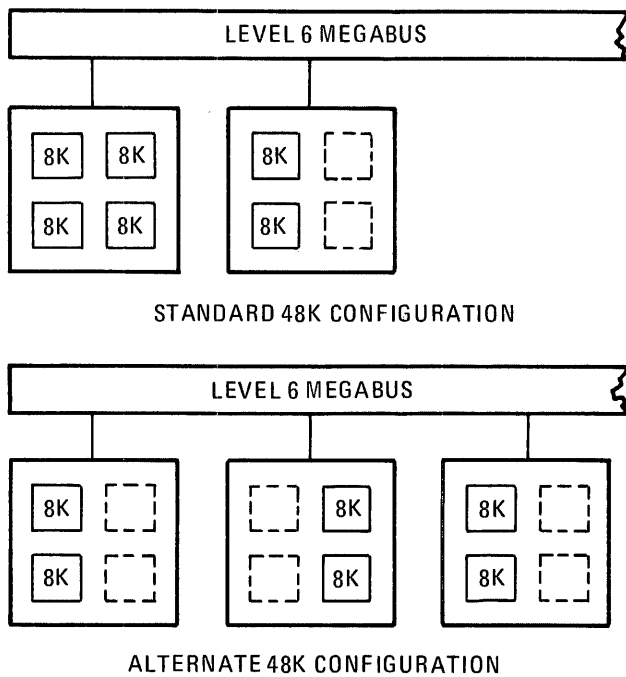
Figure 2-2. Memory Configurations

first with 32K, the second with 16K. However, the second method of putting 16K on each of three boards is allowable as long as the physical modules on the first two boards do not occupy the same positions. In this case, the same address will be set in each of the first two boards, and a different address set in the third.

Input/output controllers are used to control one or more peripheral devices or communications lines. A multiline communications controller can, for example, handle up to 8 full-duplex lines or 16 simultaneous input/output paths. Each path is considered to be a *channel* and will have a unique *channel address*. The logical capacity of the system is 1024 channels. Every device will have at least two channels assigned to it, even though both are not always used. Odd numbered channels are used for output devices, even numbered channels for input devices. Thus a line printer requires two channel addresses, but only the odd numbered channel will be used. Two diskette units on a single controller would have four channel numbers assigned, one for each device in each direction.

The channel number for each data path is a ten bit value. Of these the high-order bits are factory assigned by means of an adjustable rotary switch which is easily field changeable. The low order bits identify the "port" on the controller, with the least significant bit being the direction bit,

odd for output, even for input. A typical MDC device channel number is shown below.

Switch Selectable On Controller	Port No.	D

↑
Direction Bit
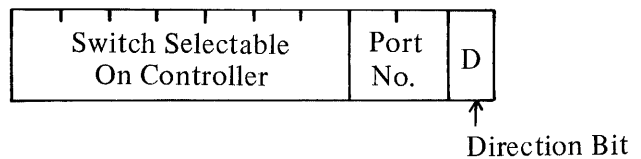
Multiple devices of the same type can thus be assigned to different channels. Channel numbers are a means of addressing input/output units and have nothing to do with either bus priority or interrupt priority levels. These are explained below.

INTERUNIT COMMUNICATION

If a processor wants to store a word in memory, it sends that word together with its memory address down the Megabus to the memory. In this case, it acts as the *master* and the memory acts as the *slave*. The transfer of the information from a master unit to a slave unit takes a single *bus cycle*. There are several types of bus cycles, and various units can become masters and various units slaves. The bus cycle described above is called a *write cycle* and is pictured in Figure 2-3.
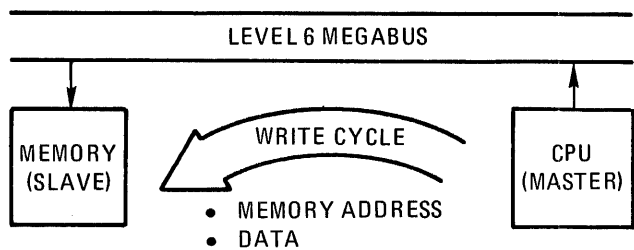
Figure 2-3. Write Cycle

The bandwidth of the bus is 6 million bytes per second, a bus cycle taking approximately 300 nsec. The bus is asynchronous in design, permitting units of varying speeds to operate efficiently on the same system. The extremely high speed of the bus allows a great many operations to be multiplexed, thereby giving a high degree of overlap between various system elements.

Megabus Priority
Any unit on the Megabus can become the master. To do so, it must have a higher priority than any other unit simultaneously also trying to become a master. Bus priority is dependent upon the relative position of the unit on the bus.

Memories have the highest priority, intervening units have lesser priority, and the central processor has the lowest. While this is shown in the diagrams as the highest priority on the left, in actuality the memories are physically at the bottom of a unit and the central processor is at the top. Therefore, the highest priority devices are those toward the bottom. See Figure 2-4.
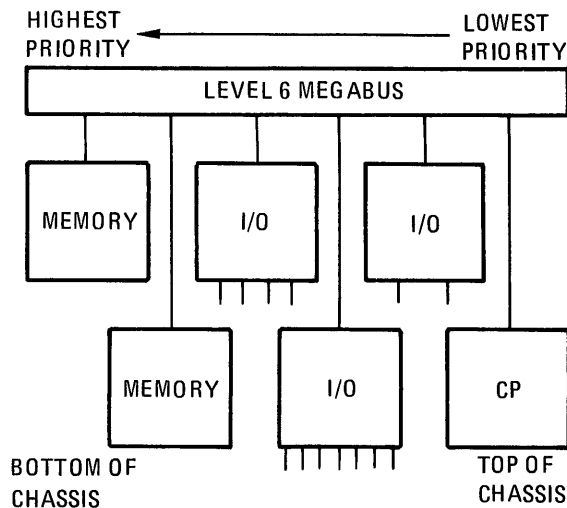
Figure 2-4. Bus Priority

Types of CP and Memory Transfers

The write cycle shown in Figure 2-3 is one type of transfer between a central processor and memory. A write requires a single bus cycle. Another common operation is when the central processor wants to read a word of data from memory. This occurs during either an instruction fetch or an operand fetch. A read operation requires two bus cycles: a *read request cycle* and a *read response cycle*. During a read request cycle, the central processor is the master and the memory the slave. The central processor sends a memory address plus its own processor ID to the memory. Accompanying this transfer is a signal that says a response is requested. Upon receipt of this request, the memory accesses data and initiates a response cycle. For this cycle the memory becomes the master and the CP becomes the slave. The memory puts the data together with the central processor address on the bus, and the CP accepts it (see Figure 2-5).

This is a typical two cycle operation. Both units will appear busy to any other unit that tries to address them during this time — with the exception of the central processor, which can accept interrupts from other units between the read request and the read response bus cycles.

The memory does not initiate the read response cycle until after it has accessed the data.
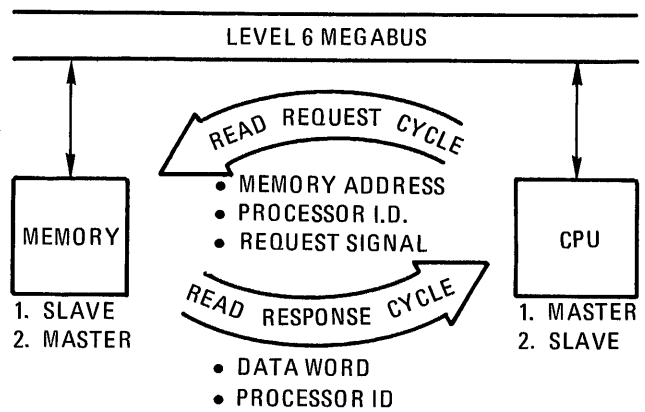
Figure 2-5. Read Operation

This is done during a 650 ·nanosecond memory cycle which partially overlaps the two bus cycles (see Figure 2-6). During this time the bus is free to accept requests from other units, interleaving bus cycles and effectively overlapping operations.
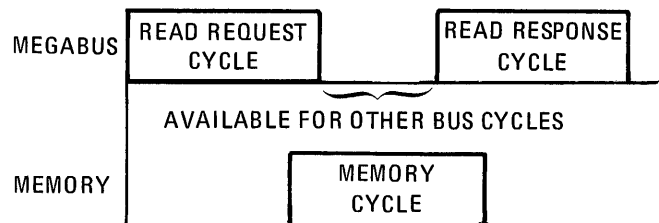
Figure 2-6. Timing of Memory Read Operation

Certain central processor to memory operations operate in read-modify-write mode and require three cycles: a read request, a read response, and a write cycle. Among these are a group of central processor instructions specifically designed to support future multiprocessor operation in that initiation of these instructions *locks* memory for the full three cycles.[1] This feature allows one processor to set flags in memory to be tested by another processor, without the chance of the second processor disturbing the flags while the process is taking place.

Input/Output Transfers

All I/O transfers on 6/30 systems occur in *direct memory access* (DMA) mode. Once a channel is set up by the central processor, data transfers are effected via the bus independent of the central processor. When a channel wants to input a word to memory, it becomes the master and initiates a write cycle transmitting the data

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[1]The six CP instructions that "lock" memory are INC, DEC, LBF, LBT, LBC, and LBS. See Section 4 for details.

and the memory address to the memory (Figure 2-7). If the channel is connected to an output device and it wants to receive a word from memory, it initiates a read request cycle and then, after the memory has accessed the data, a second bus cycle, the read response, is initiated with the memory as master and the channel controller as slave (Figure 2-8).
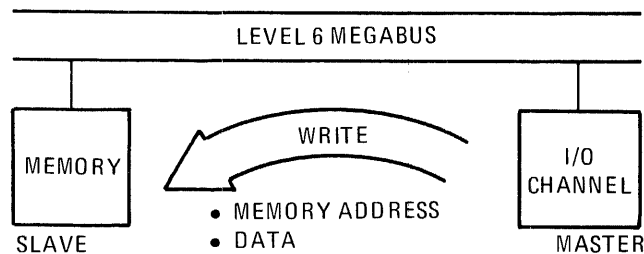
Figure 2-7. I/O DMA Input Operation
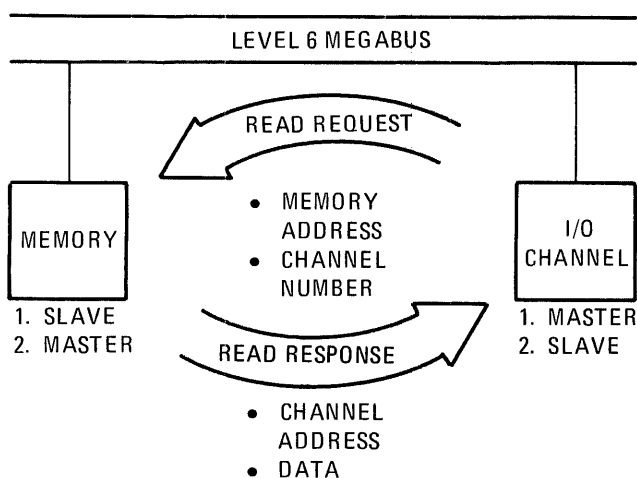
Figure 2-8. I/O DMA Output Operation

Multiple I/O units (including those on the same controller) can be operating simultaneously and can multiplex on a word basis to the same memory as long as the combined data rates do not exceed the maximum memory transfer rate of 1.67 million words per second. As this rate is approached the central processor will be locked out since I/O channels have a higher bus priority than the CP. If a second (or third) memory controller is added, true overlap can be attained, with the central processor talking to one memory unit at the same time as the input/output channel is talking to the second memory unit.

Input/Output Commands

In order for an input/output channel to initiate a DMA block transfer, it must first be set up by a central processor. This is done via an *I/O output command*. The central processor sends several words of information to the I/O controller, taking a single write cycle to send each word (see Figure 2-9). The processor sends a word of information together with a channel address and a function code defining what that word of data is. Typical words that must be sent from a central processor to a controller are *task* words identifying the operation to be performed, *configuration* words showing such things as the track and sector of a disk file, *address* words showing the address in memory where the transfer is to start, and *range* words showing how many words or bytes of data are to be transferred.
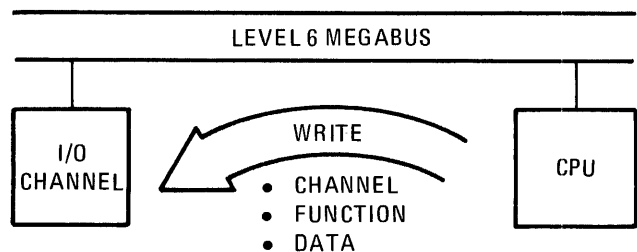
Figure 2-9. I/O Output Command

In addition to I/O output commands, the processor can initiate *I/O input commands*. These are two-cycle operations in which the processor issues a read request to the I/O channel, sending it both a channel address and a function code, plus its own processor ID. The read response cycle is then initiated by the channel, with the contents of a particular channel register being sent back to the central processor. Typical registers which are read by the processor are *status* registers showing status and error information, *range* registers typically read after a DMA transfer to determine how many characters have been read in, and *identification* registers showing a fixed ID for a particular device type. The latter allows the software to identify exactly what type of device is on a particular channel.

The two cycles of an I/O input command are shown in Figure 2-10.

Interrupt Levels

One I/O *output* command in particular is important at this point. This is the *output interrupt control* function. Utilizing this command a processor can assign an *interrupt level* to a

```
                                                    exception. It can be received by the central
┌────────────────────────────────────────┐          processor at any time, including the time between
│             LEVEL 6 MEGABUS             │          the two cycles of a read operation, although it
└────────────────────────────────────────┘          will not be processed until the instruction is
                                                    complete.
```
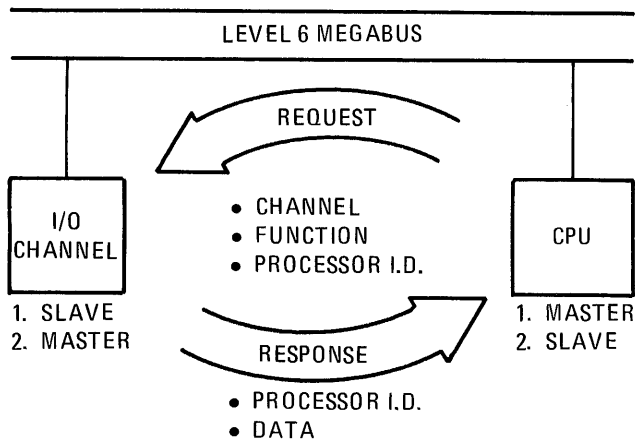
Figure 2-10. I/O Input Command

Figure 2-11. Interrupt Cycle

particular channel. There are 64 interrupt levels in 6/30 systems. Any channel can be assigned any interrupt level by the central processor. Several can have the same interrupt level if necessary. To assign an interrupt level the processor executes an I/O output command which transmits a data word containing the interrupt level and the CP channel number to the channel. This then becomes the interrupt level at which that channel may in the future interrupt. It should be noted that priority levels are thus software assigned and are completely independent of physical position.

Interrupt Commands

When a channel wants to interrupt because of a certain condition in the controller (typically the end of a block transfer), the channel initiates an *interrupt cycle* (see Figure 2-11). In this cycle, it places on the Megabus its channel number and its interrupt level and attempts to transmit these to a processor (not necessarily the same one) which had previously set up the interrupt level. A register in the processor (the S register) defines the priority level at which the processor is currently operating. Priority levels are assigned such that Level 63 is the lowest priority and Level 0 is the highest priority. If the level number of the interrupting device is numerically lower (higher priority) than the level of the central processor, an interrupt will occur. If not, then the central processor will reject the interrupt and no more interrupt cycles will be placed upon the bus by the I/O channel until it receives a signal from the central processor stating that the priority level of the central processor is changing and that it should thus reinitiate the interrupt request.

Normally a central processor cannot receive any bus signals between the time that it issues a read request and the time that it receives a read response bus cycle. An interrupt request is an
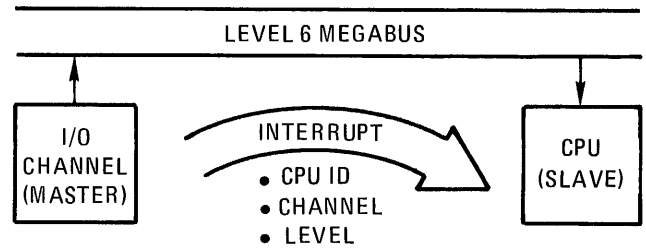
Interrupt Action

When an interrupt is accepted, the central processor assumes the level of the interrupting source. It remains at this higher priority level until interrupted by some still higher priority level, or until the CP finishes the interrupt routine and issues an instruction (the LEV instruction) that returns control to either the previously interrupted level or to an intervening level that had previously requested an interrupt cycle but had been rejected.

Consider the following (see Figure 2-12):

1. Processor running at level 40 sets up devices A, B, and C at interrupt levels 20, 30, and 25, respectively.
2. Device B requests interrupt and is accepted. Processor now runs at level 30.
3. Device A requests interrupt and is accepted. Processor now runs at level 20.
4. Device C requests interrupt but is not accepted. It will not try again until processor changes levels.
5. Processor finishes processing level 20, issues LEV instruction. This allows C to request interrupt again; it is now accepted and processor runs at level 25.
6. Processor finishes processing level 25, issues LEV instruction; no higher interrupts are pending, so it resumes level 30 processing.
7. Processor finishes level 30, issues LEV, goes back to original level 40.

Context Switching

Each interrupt level has its own individual context save area pointed to by a dedicated vector. Upon interrupt, CP firmware automatically stores the contents of all active registers in the context save area of the interrupted level and loads the registers as specified by the interrupting
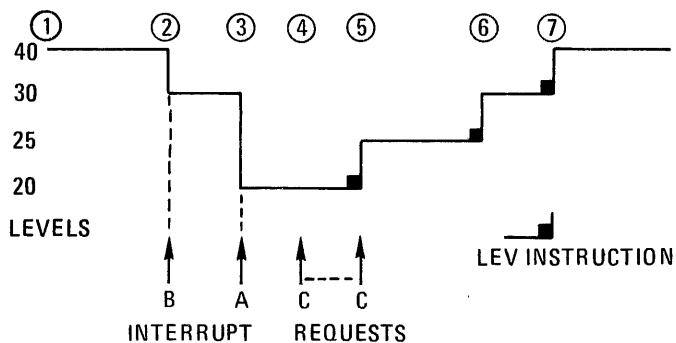
Figure 2-12. Interrupt Action

level. The number of registers whose context is saved and restored is under the control of a mask for each interrupt level, with the mask being set up by the software. Thus anywhere from 2 to 18 registers may be automatically switched upon initiation of a new level. For details on registers and the action of interrupts, see Section 3.

Summary of Bus Operations

Figure 2-13 summarizes the various Megabus operations described. The Megabus itself contains 51 information signals, which break down as follows:

24 address bits
16 data bits
 6 control bits
 5 integrity bits

There are also 17 other lines used for timing and other functions. Data lines typically hold a 16 bit data word or, on data requests, the "return address" of the requesting channel. The address lines contain either the channel number of the destination or a memory address; one of the control lines is used to differentiate which. It should be noted that memory addresses are not used to specify registers in various I/O channels. The latter are specified by a 10-bit channel

Figure 2-13. Data and Address Bus Formats

number and a 6-bit function code, leaving the full range of possible memory addresses to be utilized for addressing memory. A 32K system will have all 32K words of memory addressable.

MEMORY ADDRESSES

The basic unit of addressing in Model 6/30 systems is a word. The 6/34 and 6/36 have 16-bit program counters, 16-bit base (address) registers, and 16-bit absolute addresses within instructions. These 16 bits are used to address *words* in memory, and thus the direct addressing capability of 6/30 systems is 64K (65,536) words.

The Level 6 Megabus has 24 address lines utilized to address memory to the *byte* level. Thus, the Megabus has an architecture that is "open-ended" in that it can support processors with a direct addressing capability of over 16 million bytes. Seventeen of these lines are actually used by 6/30 systems. On word addresses, the least significant bit is zero, and thus only 16 bits need be generated by the processor.

Many instructions executed by the processor are *byte instructions*, which can generate either 16 bit addresses or 17 bit addresses. A 16 bit address will always address the left-hand byte in a memory word; a 17 bit address can address either the left-hand byte or the right-hand byte, depending on whether the least-significant (17th) bit is 0 or 1. A 6/30 system can address 128K (131,072) bytes.

Seventeen-bit byte addresses are generated in the central processor through the use of indexing. A byte count in an index register is shifted one place to the right before being added to a 16-bit word address. Thus, if an index register contained the quantity 5 and a word address of 1000 was specified, the fifth byte (starting at zero) would be selected from the left half of word 1000, or the right byte in word 1002 (see Figure 2-14). Notice that byte addresses are sequential (left to right) in memory and that data is thus in its correct sequence.*

A similar scheme is used with *bit instructions* to address bits; in this case a bit count is shifted four places to the right prior to being added to a word address.
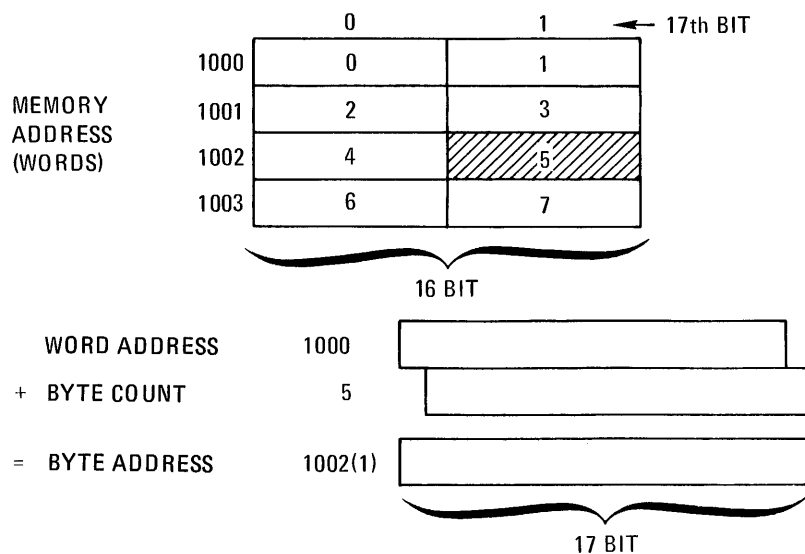
Figure 2-14. Byte Addressing

SECTION 3

CENTRAL PROCESSOR ARCHITECTURE

This section describes the architecture of the 6/34 and 6/36 central processors. From a functional point of view both processors are identical. The differences between the machines are in the amount of memory they can address, and in the number of peripherals each is capable of handling. For the purposes of this discussion they will be treated as one and the same.

REGISTERS

There are 18 registers visible to the programmer:

- 7 general registers (R1-R7); 3 can be used as index registers (R1-R3)
- 7 address registers (B1-B7)
- 1 program counter (P register)
- 1 system status register (S register)
- 1 mode control register (M1 register)
- 1 indicator register (I register)

Details on the function and operation of these registers are given in the sections that follow. All these registers can be modified via the control panel. Three other registers can also be accessed from the control panel:

- instruction register
- memory address register
- memory data register

See Section 5 for control panel operation.

Finally, there is a single 32-bit scientific register that is simulated by software and is used to store floating point operands. This register is utilized by the scientific instruction set that is automatically trapped to software routines in 6/30 systems.

DATA FORMATS

The word length in 6/30 processors is 16 bits. All hardware registers are 16 bits in length except for the M1 register, which is an 8 bit register.

Within this framework the central processor has the ability to process *doublewords* (32 bits in length), *words* (16 bits), *halfwords*, or *bytes* (8 bits), and single *bits*.

Basically there are two types of data: *signed data*, used in arithmetic operations; and *unsigned data*, used for logical quantities, addresses, ASCII characters, or any other type of internal data coding.

Unsigned data is usually expressed in hexadecimal notation. Thus a 16-bit address can range from $(0000)_{16}$ to $(FFFF)_{16}$. The contents of a byte can be expressed from $(00)_{16}$ to $(FF)_{16}$. A 16-bit word can contain two ASCII characters; if a word contained $(4139)_{16}$, this would represent "A9" in ASCII.

Arithmetic (signed) data is represented in two's complement notation. All arithmetic is performed in binary, with single word (16 bit) values extending from -32,768 to +32,767. A signed value in a byte can range from -128 to +127. Figure 3-1 shows the various data types for both signed and unsigned data.

A byte in memory can represent either an unsigned 8 bit quantity or an arithmetic value with a sign and seven bits. The byte can occupy the left- or right-hand half of a word. However, when the byte is loaded into a register, it will occupy the right half of the register. The left half will contain either zeros if a logical load instruction was used, or the sign extended if an arithmetic load was used. See Figure 3-2 for examples.

Floating point values occupy two words. The format for a floating point value is as follows:

C	S	M
0 6	7	8 31
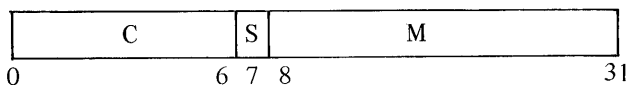
Where C is a 7 bit value representing the characteristic expressed as an excess-64 power-of-sixteen exponent.

S is the sign of the mantissa

M is the magnitude of the mantissa

GENERAL REGISTERS

There are seven *general registers* (R-register) in Model 6/30 central processors. These registers are numbered R1 through R7. It is possible to load these registers from memory either a word or a halfword at a time. It is possible to store them in memory either a word or a halfword at a time. (If a halfword store is done, it is the right half of the register that is stored.) It is possible to load and store two of them (R6 and R7) as a single doubleword. It is possible to shift each register individually or it is possible to shift them as pairs

SIGNED DATA (TWO'S COMPLEMENT)   RANGE

DOUBLE-WORD

WORD

BYTE

UNSIGNED DATA

WORD

BYTE

BIT
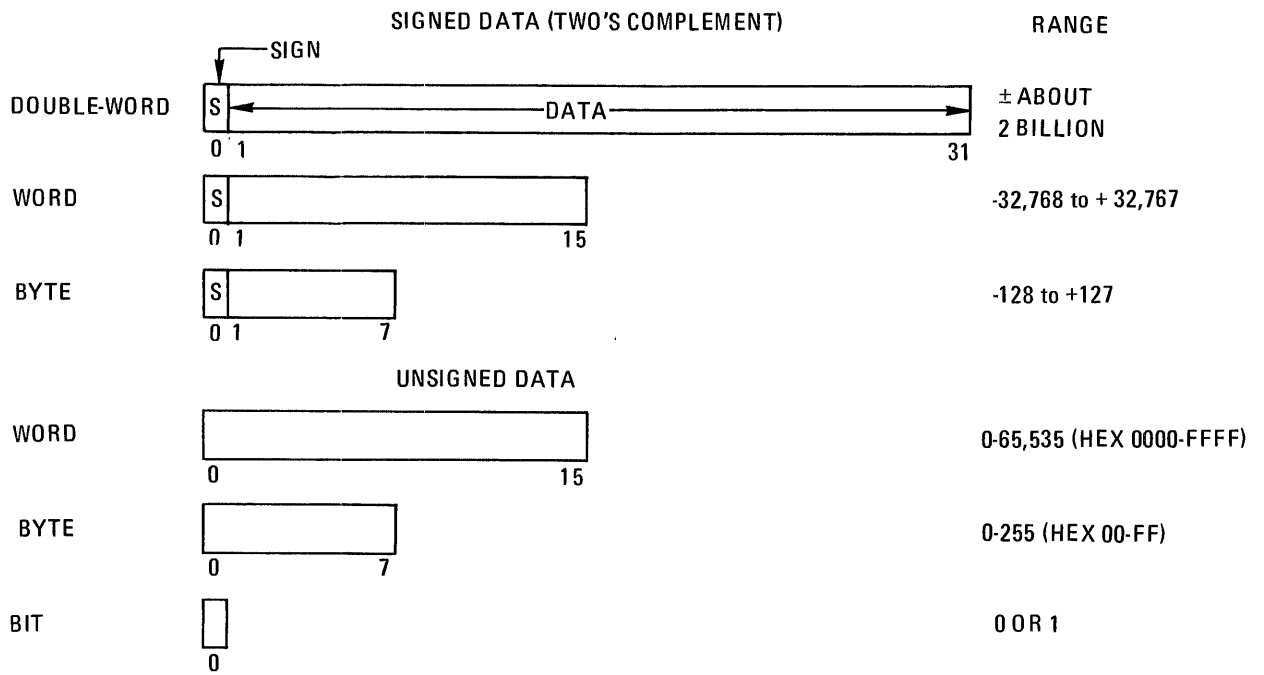
Figure 3-1. Data Formats
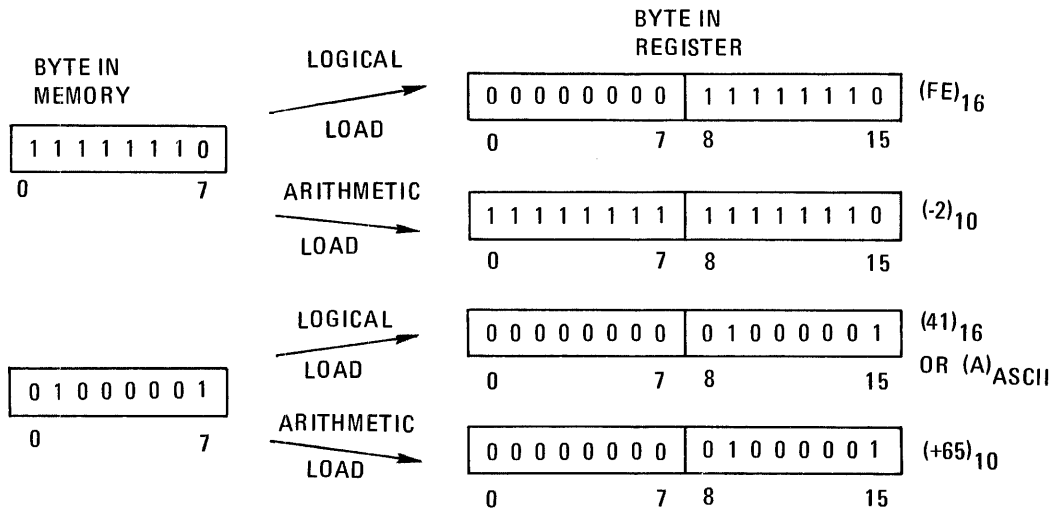
Figure 3-2. Byte Formats

(even/odd pairs) and it is possible to use these registers as operands in arithmetic, logical, and compare operations. In addition, the first three registers (R1 through R3) also double as *index registers* and may be used to store doubleword, word, halfword, or bit counts. These quantities are used to modify the addresses of words in memory. See Figure 3-3.
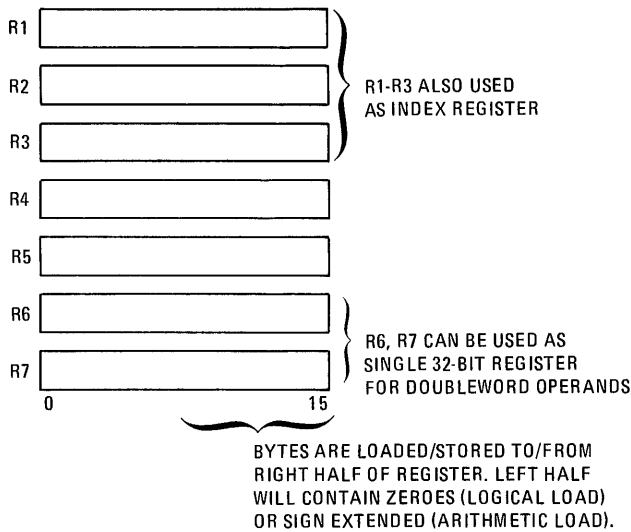
Figure 3-3. General Registers

ADDRESS REGISTERS

In addition to the seven general registers in 6/30 systems, there are seven address registers. These are also known as *base registers* and are numbered B1 through B7. It is a very important concept of Level 6 architecture that the general (R) registers are separate from the address (B) registers. While in the implementation of 6/30 systems both types of registers are 16 bits in length, it will be possible on future models to have the B-registers twice as long, thus taking advantage of the full addressing capability of the Level 6 bus.

The seven base registers can be used for formulating addresses by pointing to any procedure, data, or arbitrary location in the system. Address registers will typically contain addresses and are not used for arithmetic calculations. However, they do have the capability of being automatically incremented or decremented during instruction execution. This allows them to be used to scan arrays either forwards or backwards and also allows 6/30 systems to conveniently utilize stacks.

Details of how base registers are used in formulating addresses are given later, in the addressing techniques section below. Addresses in 6/30 systems are normally expressed as four hexadecimal digits, with the memory addresses running from 0000 through FFFF.

PROGRAM COUNTER

The program counter, or P register, is a 16 bit register that points to the next instruction to be executed in 6/30 systems. Instruction length is variable. The majority of instructions are one or two words in length, but certain instructions can be as long as six. The program counter is always incremented during instuction execution to point to the next sequential instruction. Thus, for example, if a two-word instruction is executed, the program counter will be incremented by two during its execution.

INDICATOR (I) REGISTER

This is a 16 bit register that contains various single-bit indicators. The register format is as follows:
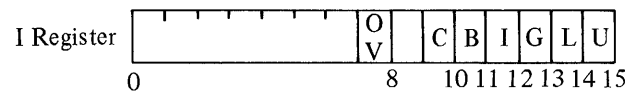
The indicators contained in this register can be grouped as follows:

- Arithmetic indicators
    OV — overflow indicator
    C   — carry bit
- Comparison indicators
    G — greater than indicator
    L — less than indicator
    U — unequal signs indicator
- Bit indicators
    B — bit test indicator
- I/O Indicator
    I — input-output indicator

ARITHMETIC INDICATORS

Two indicators are affected by arithmetic and shifting operations: the *overflow* (OV) indicator and the *carry* (C) indicator. The overflow indicator will be set when any of the seven general registers "overflows," that is, when an arithmetic result produced is larger than the capacity of the register. For example, adding the quantity 1 to a register that contains +32,767 $(7FFF)_{16}$ will set overflow because the *arithmetic* capacity is exceeded. The register would contain $(8000)_{16}$, or -32,768 after the addition. If the data were not to be interpreted as signed data, the overflow could be ignored.

The *carry* (C) indicator, conversely, is set when the *logical* capacity of a register is exceeded. Thus if 3 were added to a register that contained $(FFFE)_{16}$, a carry to the 17th bit would be produced, i.e., the answer would be $(1)(0001)_{16}$. However, if these were arithmetic quantities, $(FFFE)_{16}$ would represent -2, and adding +3 to it would produce $(0001)_{16}$; this is the correct answer and thus the carry could be ignored.

COMPARISON INDICATORS

The three indicators which are controlled by compare instructions are the greater than (G), less than (L), and unlike signs (U) indicators. These one bit indicators contain the results of the last compare instruction executed by the computer and in turn can be tested by other central processor instructions (see branch on indicator in Section 4).

A comparison is typically executed between a register and a word in memory. If the contents of the register are greater, the G indicator will be set; if the contents of memory are greater, the register is less and L will be set.

OTHER INDICATORS

Two other indicators are extremely useful to the programmer; the (B), or bit test, indicator; and the (I), or input/output, indicator.

Bit Test Indicator

This can be considered a one bit register loaded by load bit instructions. Not only can it be loaded from any bit in any word of memory, but it can also be set if any of a group of bits in a word in memory is set. The selection is done under the control of a 16 bit mask and is very useful for testing bit patterns in memory.

Input/Output Indicator

The I bit serves to store an indication of whether the last input/output command was successful. For example, if the central processor issues a command output to a peripheral channel that is busy, the peripheral channel will issue a "NAK", which in turn will cause the I/O indicator to be set. Software can then test this indicator and determine what alternate action to take.

M1 REGISTER

Another control register is the mode control register, or M1 register. This is an eight-bit register that controls whether certain conditions will cause traps or not.

M1 Register

Overflow trap control bits
Trace trap control bit
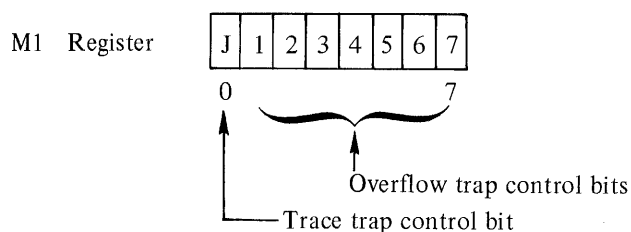
The seven overflow trap control bits are associated with the seven general registers, R1-R7. If overflow in any one of these occurs and if the corresponding trap control bit is set, a trap will occur through trap vector 6. This facility saves the programmer from having to test the result of every arithmetic operation for overflow, and yet also guarantees that overflow will not go undetected.

The other bit in this register, bit zero, is the trace trap enable bit, also known as the J bit. When this is enabled, all jumps and branches that are executed in a program will cause a trap to the trace entry location. This bit therefore allows a programmer to trace a code without having to modify its procedure at all.

S REGISTER

The third control register in Level 6/30 systems is a 16 bit register known as the S register, or status register. This register contains three fields, as shown below: the privileged state indicator (P), the interrupt priority level, and the processor ID.
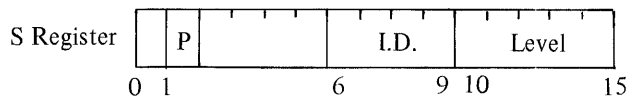
S Register

PRIVILEGED STATE INDICATOR

There are two modes of instruction execution on 6/30 systems — user mode and privileged mode. The privileged bit in the S register defines this mode. If it is not set, the processor is in the user mode and will automatically trap when certain instructions are attempted. Input/output command instructions plus the interrupt level change instruction are privileged instructions and can be executed only when the privilege mode bit is set. They will be automatically trapped if attempted in user mode. By utilizing this hardware feature, systems can be protected against unauthorized use of input/output by user routines.

PRIORITY LEVEL

The 6 bit level contained in the S register defines the priority level on which the processor

is currently executing instructions. Upon interrupt requests from other units, it also determines whether the interrupting unit is of higher, equal, or lower priority. Only higher priority interrupt requests are granted. When an interrupt occurs, the level of the interrupting unit replaces the level in the status register of the interrupted level. The old level is always automatically stored. See the section on interrupts below for further details of this operation.

PROCESSOR ID

This is a 4 bit field that is fixed during system configuration. It is typically zero (a second processor in the system would have an ID of 0001). These 4 bits are used as the four least significant bits of the 10 bit channel number for the processor itself. The high 6 bits are always zero. Thus, the processor ID and the processor channel number are for all intents and purposes synonymous.

The processor ID in the S register is hard-wired and cannot be changed under program control.

SUMMARY OF PROGRAM VISIBLE REGISTERS

Thus 18 registers are visible to the programmer: seven general registers (R1 through R7), seven address registers (B1 through B7), one program counter (P register), and three control registers — the S register (status), the I register (indicator), and the M1 register (mode control register). These are shown in Figure 3-4. Of the 18 registers, two are automatically saved and restored upon interrupt (the S register and the P register). The other 16 have their context stored and restored under firmwave control according to a 16 bit mask. This mask, which is also used by the save context (SAVE) and restore (RSTR) instructions, is set up under program control. Its format is as follows:

Interrupt Save Mask

ISM	M1	R1	R2	R3	R4	R5	R6	R7	I	B1	B2	B3	B4	B5	B6	B7

INTERRUPTS

There are 64 levels of interrupt, numbered from 0 to 63; level 0 has the highest priority Clearing the computer puts it into level 0, which in effect makes it uninterruptable.

Associated with each interrupt level is a dedicated memory location that contains the interrupt vector. These locations, extending from address 0080 to address 00BF, contain a pointer to an interrupt save area. The interrupt save area needs only to be set up by those levels which are active in a particular program. Each interrupt save area has five fixed locations and up to 16 more variable locations. These locations are as follows:

1. DEV — in this location the channel number and device ID of the interrupting device are automatically stored.
2. ISM — this location contains the interrupt save mask (see above). This mask controls which of the 16 registers will be saved in the variable portion of the interrupt save area.
3. Reserved for future use.
4. P — in this word the program counter of the interrupt level is stored. It also acts as a pointer to the interrupt handling procedure for a new level, or upon restoration of an interrupted level, to the location of the next instruction to be executed.
5. S — this is where the status register is automatically stored. Note that when a new interrupt level is set up, the S register is loaded from this location only as far as the privileged mode bit is concerned; the level is generated automatically, and the processor ID is hardwired.
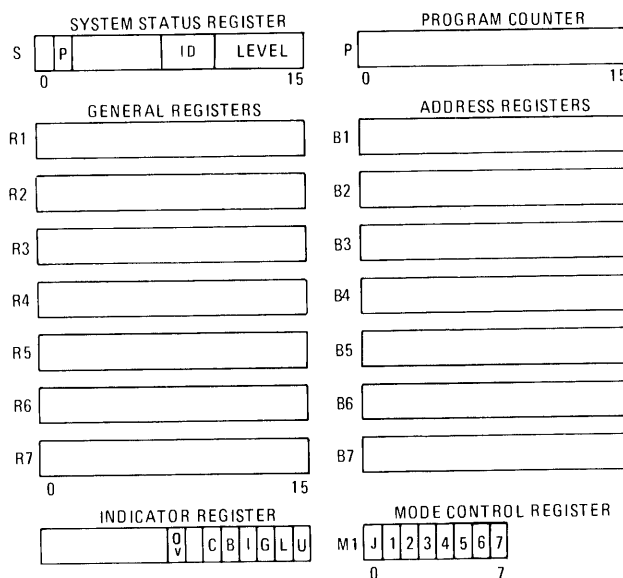
Figure 3-4. Register Complement

Words 6-21 are locations for saving the 16 machine registers under control of the interrupt save mask. If the interrupt save mask is all zeros, none of these words will be reserved.

The sequence of storage is as specified in the interrupt mask from right to left, that is, B7 first and M1 last.

It should also be noted that the word prior to the one pointed to by the interrupt vector, that is, the word prior to the device word, is also a dedicated word. This is called the TSAP and points to a trap save area. See discussion of traps below.

Figure 3-5 shows this action of an interrupt. Both levels 20 and 30 have had their interrupt save areas set up — level 20's at AB20, as pointed to by its vector at 0094; and level 30's at 1000, as pointed to by its vector at 009E.

If level 30 is interrupted by level 20, firmware automatically saves the register contents in the level 30 interrupt save area and loads the register with the values in the level 20 interrupt save area. One of these values is the starting address of the level 20 interrupt subroutine which is automatically loaded (in this example) from location AB23 into P.

Associated with each interrupt level is a dedicated flag bit which is set when the interrupt is initiated. These bits are stored in four dedicated memory locations, 0020-0023. In the example above, both bits 20 and 30 would be set. At the end of the interrupt routine for level 20, a level change instruction (LEV) would be executed. This would clear the bit for level 20 and then scan the table to determine which was the next highest scheduled level. If no intermediate interrupts (such as level 25) were pending, it would scan the table, find bit 30 set, and therefore return to level 30.

The LEV instruction can set or reset activity flags, change the current level, inhibit interrupts, or do a "quick change" without saving and restoring context. By changing the current level to level 3 all device interrupts can be inhibited; level 2 (overflow of trap context scan area), level 1 (watchdog timer runout), and level 0 (incipient power failure) will still be enabled. Table 3-1 shows the assignment of interrupt levels.

TRAPS

Traps are caused by events such as overflows, parity errors, addressing non existent resources, or executing a scientific instruction. A trap can occur at any priority level, and several can be nested at the same level. A trap could be entered at one level, that level interrupted during the execution of the trap routine, and then the same trap routine reentered in the new level. See Table 3-2.

TABLE 3-1. EVENT INTERRUPT LEVEL ASSIGNMENT

Event Causing Interrupt	Level Assignment	Comment
Incipient Power Failure	0	Highest priority
Watchdog Timer Runout	1	–
Overflow of Trap Context Save Area	2	–
Real Time Clock	–	Level is contained in main memory location 0016 (HEX)
Device Requiring Service	–	Level is either fix wired or dynamically controlled by software
LEV Instruction	–	Level specified in instruction

TABLE 3-2. TRAP VECTORS AND EVENTS

Vector #	Event
Vector #1	Monitor call (MCL instruction)
Vector #2	Trace (debug) or BRK instruction
Vector #3	Scientific operation not in hardware
Vector #4	Reserved for future use
Vector #5	Other operation not in hardware (or undefined)
Vector #6	Integer arithmetic overflow (if enabled)
Vector #7	Reserved for future use
Vector #8	Reserved for future use
Vector #9	Reserved for future use
Vector #10	Reserved for future use
Vector #11	Reserved for future use
Vector #12	Reserved for future use
Vector #13	Unprivileged use of privileged operation
Vector #14	Reserved for future use
Vector #15	Reference to unavilable resources
Vector #16	Program Logic Error. (RTT executed with TSAP having a NULL value.)
Vector #17	Memory error (parity non-correctable ECC) detected
Vector #18 thru Vector #46	Reserved for future use
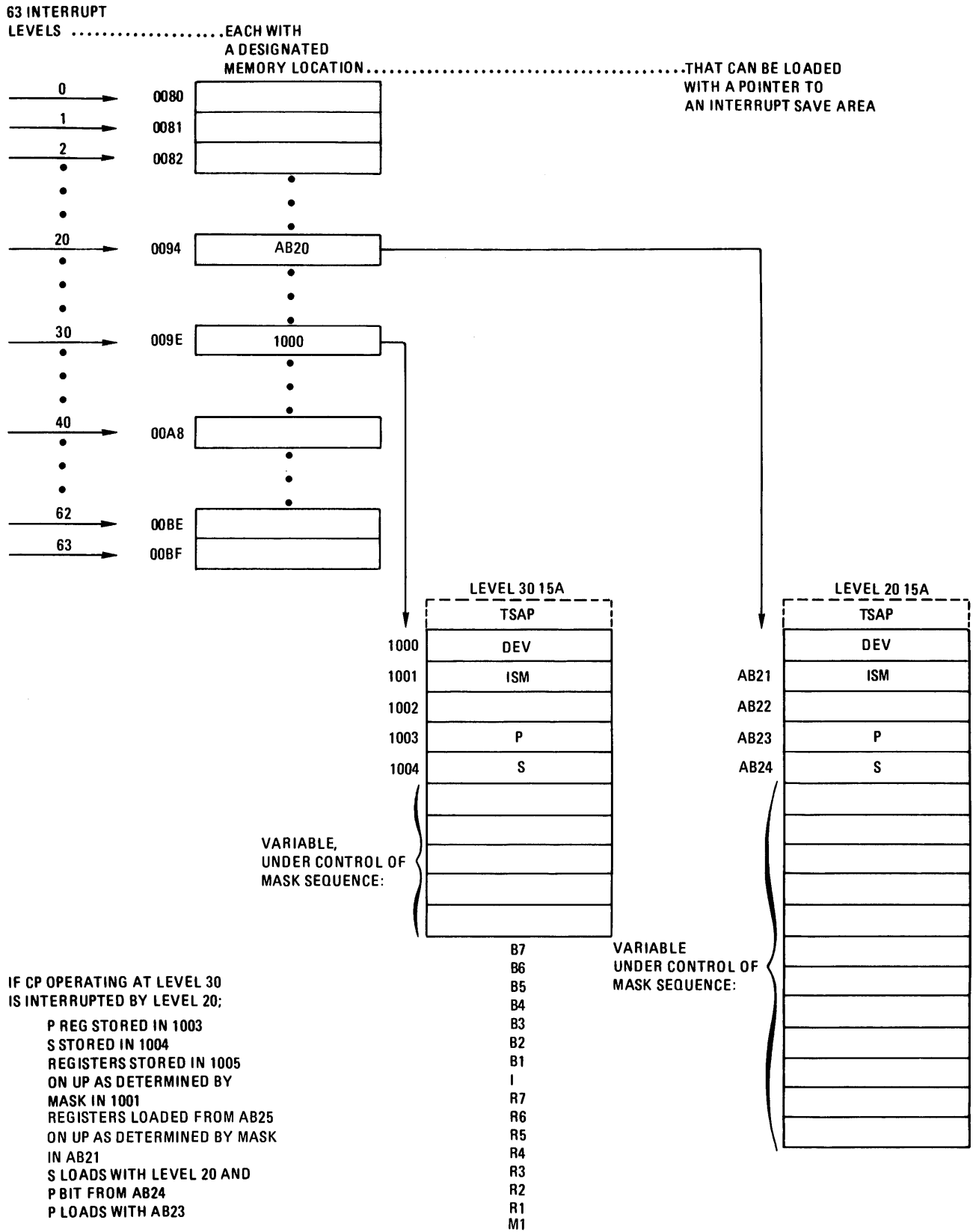
Figure 3-5. Interrupt Action

Each type of trap has its own trap vector containing a pointer to the trap handling procedure. Also utilized is a pointer in location 10 to the next available trap save area. The latter are pooled, and pointers to the next available area are automatically adjusted by firmware. Upon a trap taking place, certain, but not all, register contents are automatically stored in the trap save area. The pointer in the first word of the interrupt save area for the current level is adjusted so that it points to the trap save area; the pointer in the trap save area points to any other traps that occurred at the same interrupt level. Thus several traps may be nested at the same interrupt level. At the end of the execution of the trap-handling procedure, a return from trap (RTT) must be executed; this does a restoration of the partial context that was stored, unlinks the trap save area, and returns all pointers to their original state.

The relationship of traps and interrupts and their vector linkage are shown in Figure 3-6. The trap vector (TV) points to the trap handler procedure. The trap save areas contain the following information:

TSAL — Trap save area link
I — Contents of indicator register
R3 — Contents of register R3
Inst — The instruction causing the trap
Z — Miscellaneous information
A — The address of the instruction following the traffic instruction (not necessarily the next to be executed)

P — The program counter; e.g. on a branch the location to which the branch would go if it were not trapped
B3 — The contents of register B3.

Note that the address of this area is noted in the Trap Save Area Pointer (TSAP) in the *interrupt* save area for the current level.
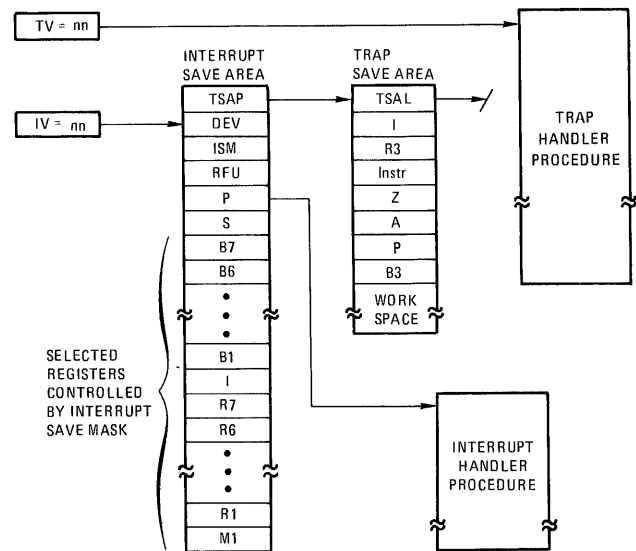
Figure 3-6. Trap Vector and Interrupt Vector Linkage

SECTION 4

INSTRUCTIONS & ADDRESSING

INSTRUCTION SET SUMMARY

The Model 6/30 instruction set consists of over 100 instructions, grouped as follows:

- Double Operand
- Single Operand
- Branch on Register
- Branch on Indicator
- Short Value Immediate
- Shift
- Generic
- Input/Output
- Scientific instruction executed interpretively

These are 'summarized below. The instruction formats for each type and the addressing modes are detailed later in this section.

1. *Double Operand* instructions are memory reference instructions in which the first operand is a register address and the second operand is usually a memory address, although for register to register instructions, the second address can also specify a register. A typical double operand instruction is an (ADD) instruction, which adds the contents of the addressed memory location (or register) to the general (R) register specified by the first operand. Thus, the instruction ADD $R1, LOC adds the contents of memory location "LOC" to register R1[1].

2. *Single Operand* instructions can address memory (or a register) in the same way as double operand instructions, but they do not need a register address. A typical single operand instruction is the Clear (CL) instruction, which clears the addressed memory location to zero. In assembly notation, this instruction could be written as follows: CL LOC.

3. *Branch on Register* instructions are similar to double operand instructions in that they must specify a general register, R1 through R7, and also a memory address to which control will be transferred if the tested condition is true. A typical branch on register instruction is Branch if Register Odd (BODD), which might be written as follows: BODD $R6, LOC. This would test register 6 to see whether it were even or odd, and if it were odd the program would branch to location LOC.

4. *Branch on Indicator* instructions are similar to branch on register instructions, but the op code specifies an indicator and no register address is required. A typical instruction is Branch if Greater than (BG), which will branch if the G (greater than) indicator is set. This will be written as follows: BG LOC.

5. *Short Value Immediate* instructions do not reference memory but specify a register and an 8-bit immediate operand which is contained in the instruction itself. For example, if it were desired to add the quantity 2 to register R3, the Add Value (ADV) instruction could be used. This would be written as follows: ADV $R3, =2.

6. *Shift* instructions are used to shift either single general registers or pairs of general registers. The first operand specifies the register itself or, in the case of a double word shift, the right-hand (odd) register of a pair. The second operand usually specifies the number of positions to be shifted. A typical shift instruction is shift closed left (SCL), which rotates the contents of a register "n" positions to the left. For example, to rotate R6 four places to the left, the following instruction would be used: SCL $R6, 4. To rotate both 6 and 7 together, a double closed left would be utilized: DCL $R7, 4.

7. *Generic* instructions have no variable addresses and need only an op code. Typically, these are control instructions. A typical instruction in this group is Monitor Call (MCL), which generates an automatic trap via vector 1.

8. *Input/output instructions* enable the processor to communicate directly with input/output channels by sending the channel either an output command or an input command request (see Section 2). A typical I/O command is the I/O load (IOLD) instruction, which sends *both* an address and a range to the addressed channel. Thus, this

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[1] Instruction examples will be given in Assembly Notation. For details, see the Level 6 Assembly Language Manual, Order No. AS31.

instruction has three operands and could be written as follows: IOLD ADDR, CHAN, RANGE. This instruction in machine language, depending upon the address form used, could occupy from 3 to 6 words of memory.

9. *Scientific* instructions on 6/30 systems are not implemented by hardware; the op codes cause traps to software routines.

INSTRUCTION FORMATS AND ADDRESSING MODES

Single and Double Operand Instructions

The format for single and double operand instructions is as follows:

```
0 1    3 4      8 9              15
 ┌─┬─────┬──────────┬─────────────────┐
 │1│  r# │ op code  │ address syllable │
 ├─┴─────┴──────────┴─────────────────┤
 ¦              optional               ¦
 └─────────────────────────────────────┘
```
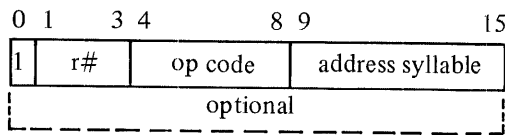
Single Operand Instruction: # bits 1-3 will be zero

Double Operand Instruction: # bits 1-3 will specify a register number from 1-7.

The significance of the bits is as follows: bit 0 is always a 1; bits 1, 2 and 3 will be 0 for single operand instructions and will define a register number (1-7) in double operand instructions (the op code will define whether this is one of the 7 general (R) registers or one of the 7 address (B) registers); bits 4 to 8 define the operation code; bits 9-15 are the *Address Syllable* and are used to define either:

- a location in *memory* that contains an operand
- a *register* that contains an operand
- an *immediate* operand, where the operand is contained in the second word of the instruction.

Single and double operand instructions can be either one word or two words in length depending on the addressing mode utilized. The addressing mode is defined by the address syllable. Instructions that address a register are one word in length; instructions that utilize an immediate operand are considered to be two words in length, including the operand, since the program counter is incremented by two in order to access the next instruction; and finally, instructions that address operands in memory can be either one or two words in length depending on the addressing mode used; these are as follows.

Absolute addressing (also called immediate address mode). These are two word instructions where the second word contains a 16-bit absolute address. This address can be

- direct address
- an indirect address
- a direct address indexed by the contents of R1, R2, or R3.
- an indirect address that is post-indexed by the contents of R1, R2, or R3.

Base addressing. These are one-word instructions that define one of the seven address registers (B1-B7) as containing the address of the operand. The address in the register can be

- a direct address
- a direct address indexed
- an indirect address
- an indirect address post-indexed.

In addition, some extremely powerful additional modes of base addressing are provided. These are still all one word instructions:

- Base, pre-decremented (also called push addressing). In this mode one is subtracted from the contents of an address register prior to its being used as an address — unless it is a doubleword load or store, in which case two is subtracted.
- Base, post-increment (also called pop addressing). Here one (or two, as above) is added to the contents of an address register after it has been used as an address.
- Base, auto-indexed. Here the contents of an index register R1, R2, or R3 are either pre-decremented (push indexed) or post-incremented (pop indexed) before/after being added to the contents of an address register B1, B2, or B3.

Relative addressing. These are two-word instructions where the second word contains an algebraic displacement ($\pm32K$) relative to either the program counter (P relative), an address register (Base relative), or the interrupt vector for the current central processor level (IV relative). The resultant address can be utilized as either a direct or an indirect address (except for IV relative, which is direct only).

Summary of Single and Double Operand Instruction Addressing Modes

Table 4-1 summarizes the addressing modes. Note the major breakdowns of register addressing,

TABLE 4-1. SUMMARY OF ADDRESSING MODES FOR SINGLE AND DOUBLE
OPERAND INSTRUCTIONS

Operand Location	Types of Addressing	Instruction Length (Words)	Assembly Example Using ADD Command
Register	Register Addressing	1	ADD $R6, =$R5
Instruction	Immediate Operand	2	ADD $R6, =1000
Memory	Absolute (Immediate Address)	2	
	• Direct		ADD $R6, <LOC
	• Indirect		ADD $R6, *<LOC
	• Indexed		ADD $R6, <LOC. $R3
	• Indirect Indexed		ADD $R6, *<LOC. $R3
	Base Addressing	1	
	• Direct		ADD $R6, $B7
	• Indirect		ADD $R6, *$B7
	• Indexed		ADD $R6, $B7. $R3
	• Indirect Indexed		ADD $R6, – $B7.$R3
	• Pre-Decrement		ADD $R6, –$B7
	• Post-Increment		ADD $R6, +$B7
	• Auto-Indexed, Pre-Decrement		ADD $R6, $B3.–$R3
	• Auto-Indexed, Post-Increment		ADD $R6, $B3. +$R3
	Relative Addressing	2	
	• P-Relative Direct		ADD $R6, LOC
	• P-Relative Indirect		ADD $R6, *LOC
	• Base Relative, Direct		ADD $R6, $B7.–5
	• Base Relative, Indirect		ADD $R6, *$B7.7
	• Interrupt Vector Relative		ADD $R6, $IV.7

memory addressing, and immediate addressing. An assembly language example for an add instruction is shown next to each mode. For further information on instruction addressing in assembly language, see the referenced assembly language manual for Level 6 systems.

Branch Instructions

There are two types of branch instructions: branch on register and branch on indicator. The format is as follows:

```
0 1   3 4      8 9       15
┌─┬─────┬─────────┬──────────────┐
│0│ r#  │ op code │ displacement │
└─┴─────┴─────────┴──────────────┘
╷         optional              ╷
└ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
```
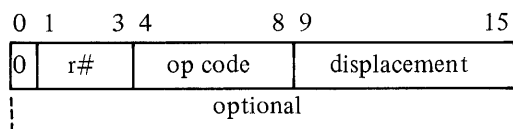
A branch on indicator instruction will have zeros in the register field, bits 1 through 3, while a branch on register instruction will have the number (from 1 to 7) of one of the general (R) registers.

These instructions again can be either single- or doubleword instructions. Three addressing modes are possible with branch instructions: displacement, relative, and absolute.

Displacement Addressing

In this mode an 8-bit displacement is contained within a one-word instruction. The displacement is a 7-bit algebraic quantity that is applied to the contents of the program counter. Utilizing this mode of addressing, the program can branch to 64 locations prior to the instruction or 63 locations after it. Displacements of zero and one are not allowed.

Relative Addressing

This mode of addressing is identical to the P-relative addressing mode in single and double operand instructions. The second word of the instruction contains a signed 16-bit value (±32K), which is applied to the contents of the program counter.

Absolute Addressing (Immediate Address)

Again this is identical to single and double operand instructions. In this mode a two-word instruction is used, with the second word containing an absolute 16-bit word address that describes a branch location from 0 to 64K.

Summary of Branch Instruction Addressing Modes

Table 4-2 shows the three types of addressing modes that can be utilized with branch instructions together with the assembler mnemonics for each.

TABLE 4-2. BRANCH INSTRUCTION ADDRESSING FORMS

Short Displacement	1 Word	BG >LOC
Long Displacement (P-Relative)	2 Words	BG LOC
Absolute (Immediate Address)	2 Words	BG <LOC

Short Value Immediate Instructions

The format for these instructions is as follows:

```
 0 1   3 4   7 8           15
+--+----+--------+-----------+
|0 | r# | op code|   value   |
+--+----+--------+-----------+
```
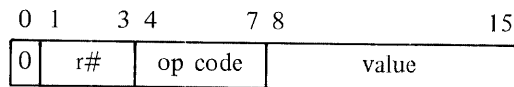
Bits 1-3 must specify a general (R) register number. Bits 8-15 contain an arithmetic value between -128 and +127. This value (with its sign extended) is used as an operand by the instructions that utilize this addressing form.

SHORT VALUE IMMEDIATE ADDRESSING FORM

Short Value Immediate   1 Word   ADV $R6, =6

Shift Instructions

Shift instructions have the following format:

```
 0 1   3 4    7 8              15
+--+----+-------+----------------+
|0 | r# | 0 0 0 0| type & distance|
+--+----+-------+----------------+
```
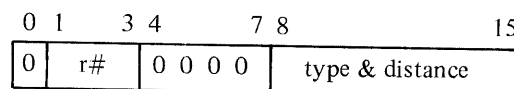
Bits 8-15 are used to specify the type, direction and number of bits to be shifted. If the number of bits field is zero, register R1 will contain the shift distances. Short shifts can specify a distance of up to 15 bits; long shifts, up to 31 bits. Bits 1-3 specify a general (R) register number. If a double shift is to be executed, this field must address the right-hand (odd) register.

ADDRESSING MODE

Short shift	1 Word	SAL $R5, 6
Long shift	1 Word	DAL $R5, 26

Generic Instructions

Generic instructions have the following format:
Bits 0-7 must be zeros, while bits 8-15 specify the function.

```
 0               7 8            15
+-----------------+--------------+
|0 0 0 0 0 0 0 0 |   function    |
+-----------------+--------------+
```
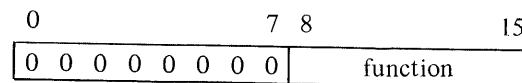
Input/Output Instructions

There are two types of input/output instructions. The first type is used by the input/output word (IO) or by the input/output halfword (IOH) instructions. This is the instruction that is used to place an I/O command on the level 6 Megabus (see Section 2). An I/O command consists of a channel number, a function on the address bus, and a 16-bit data word on the data bus. The instruction format to do this is as follows:

```
 0 1   3 4    8 9           15
+--+-------+--------+----------+
|1 |0 0 0 | op code |   DAS    |
+--+-------+--------+----------+
|        optional            |
+----------------------------+
|   channel      | function  |
+----------------------------+
 0               9 10       15
```
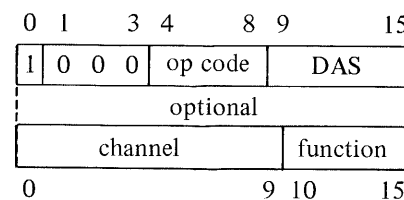
The address of the data word is defined by the Data Address Syllable (DAS) in the least significant 7 bits of the instruction and by a second word if needed. The addressing forms are the same as single word operand addressing and the second word will be needed for absolute addressing, relative addressing, or base plus deplacement addressing modes. The last word of the instruction contains the channel address and the function code. If it is desired not to embed the channel number and the function code in the procedure, then the instruction can take the following format:

```
| 1 | 0 | 0 | 0 |  op code  | DAS |
```
```
|           optional            |
```
```
| 0 0 0 0 0 0 x x x | CAS |
```
```
|           optional            |
```
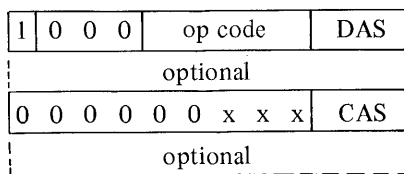
In this case the Channel Address Syllable (CAS) bits point to the location of a word containing the channel and function. Again, a second word may be required to define this address.

The second type of I/O instruction is the IOLD instruction. This is similar except that instead of placing one word of data on the I/O bus it places two words of data. These two words are specifically the address and range that are required to set up a DMA transfer. The format is the same as for the I/O instructions above, except that a third address must be specified. Again, this can be one or two words, depending upon the addressing mode utilized. The two cases are thus as follows, with the first embedding the control in the procedure and the second having the control word nonprocedural:

```
0 1    3 4         8 9        15
| 1 | 0 0 0 | 0 0 0 1 1 |  AAS  |
|           optional            |
|      channel      |  function |
| x x x x x x x x x |  RAS  |
|           optional            |
```
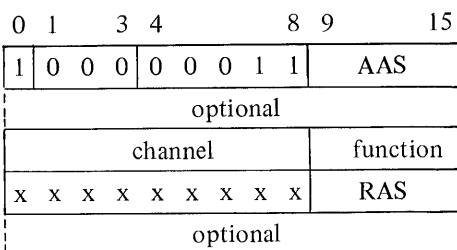
AAS – address syllable defining buffer address
RAS – address syllable defining location of range

```
| 1 | 0 0 0 | 0 0 0 1 1 |  AAS  |
|           optional            |
| 0 0 0 0 0 0 x x x |  CAS  |
|           optional            |
| x x x x x x x x x |  RAS  |
|           optional            |
```
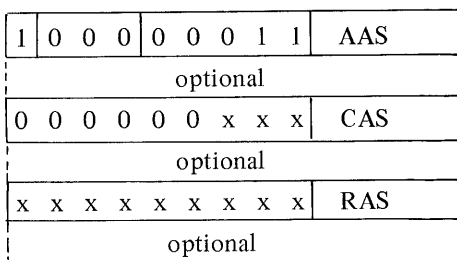
CAS – address syllable defining location of word
containing channel and function

Scientific Instructions

Scientific instructions do not have unique formats; they take the formats of either single or double operand instructions. Note that they are not executed by hardware but rather cause traps to unique software routines which execute the instructions. These instructions, described in the referenced assembly language manual, are as follows:

SAD	Scientific Add
SCM	Scientific Compare
SCZD	Scientific Compare with Zero
SDV	Scientific Divide
SLD	Scientific Load
SML	Scientific Multiply
SNGD	Scientific Negate
SSB	Scientific Subtract
SST	Scientific Store
SSW	Scientific Swap

INSTRUCTION SET

The instructions that are implemented by hardware are described in detail on the pages that follow.

ADD

Instruction:
    Add to R-register

Type:
    Double Operand

Format:

```
0 1    3 4       8 9            15
| 1 |  Rn  | 1 0 1 0 0 | address syllable |
|              optional                   |
```
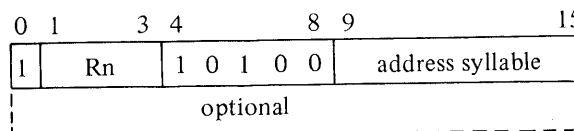
Description:
    Adds the word at the effective address to the word contained in the designated R-register. The carry (C) and overflow (OV) indicators will be set if carry and/or overflow occurs respectively; otherwise they will be reset to zero. The address syllable can specify a memory location, an immediate operand, or another R-register.
    Some examples of addition:

R-Register (Before)	Effective Address (Before & After)	R-Register (After)	C (After)	OV (After)
$+(32,766)_{10}$	+1	+32767	0	0
$+(32,767)_{10}$	+1	-32768	0	1
+1	-2	-1	0	0
-1	+2	+1	1	0
$(FFFF)_{16}$	+2	0001	1	0

ADV

Instruction:
   Add Value to R-register

Type:
   Short Value Immediate

Format:

0	1 3	4 7	8 15
0	Rn	1 1 1 0	value
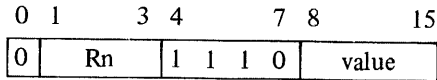
Description:
   Adds the value contained in the instruction (with the sign extended) to the designated R-register. Overflow (OV) and carry (C) indicators are set/reset according to the results of the addition.

AND

Instruction:
   AND with R-register

Type:
   Double Operand

Format:

0	1 3	4 8	9 15
1	Rn	0 1 0 1 0	address syllable
	optional		
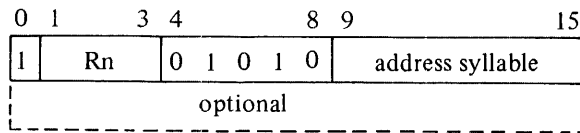
Description:
   Logically AND's the word at the effective address to the word contained in the designated R-register. No indicators are affected. The address syllable can specify a memory address, an immediate operand, or another R-register.
   The following chart illustrates the result of logically ANDing bits:

First operand bit	0	0	1	1
Second operand bit	1	0	1	0
Result	0	0	1	0

Examples:

R-Register (Before)	Effective Address (Before & After)	R-Register (After)
$(ABCD)_{16}$	$(00FF)_{16}$	$(00CD)_{16}$
$(ABCD)_{16}$	$(7777)_{16}$	$(2345)_{16}$

ANH

Instruction:
   Logically AND halfword (byte) with R-register

Type:
   Double Operand

Format:

0	1 3	4 8	9 15
1	Rn	0 1 0 1 1	address syllable
	optional		
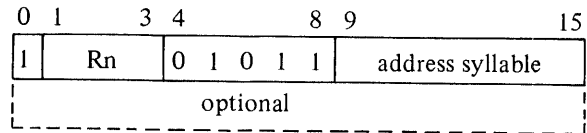
Description:
   Logically AND's the byte at the effective address (with its sign extended) to the word contained in the designated R-register. No indicators are affected. The address syllable can specify a memory address, an immediate operand, or another R-register, with the byte being positioned as follows:

   — memory location, not
      indexed   — left byte
   — memory location, indexed
      index value even   — left byte
      index value odd   — right byte
   — immediate operand   — left byte
   — R-register   — right byte

   The following chart illustrates the result of logically ANDing bits:

First operand bit	0	0	1	1
Second operand bit	1	0	1	0
Result	0	0	1	0

Examples:

R-Register (Before)	Effective Address (Before & After)	R-Register (After)
$(ABCD)_{16}$	$(FF)_{16}$	$(ABCD)_{16}$
$(ABCD)_{16}$	$(77)_{16}$	$(0045)_{16}$

B

Instruction:
   Branch unconditionally

Type:
   Branch on Indicator

Format:

```
0  1    3 4      8 9            15
┌─┬─┬─┬─┬─┬─┬─┬─┬─┬──────────────┐
│0│0 0 0│1 1 1 1 1│  displacement │
└─┴─────┴─────────┴──────────────┘
  optional
```
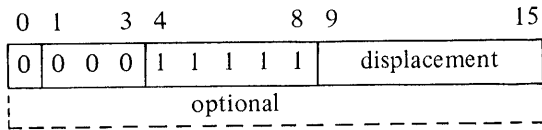
Description:

Branches to the specified location uncondition-ally unless the J bit in the mode control (M) register is set, in which case it traps to trap vector #2.

BAG

Instruction:

Branch if algebraically greater than

Type:
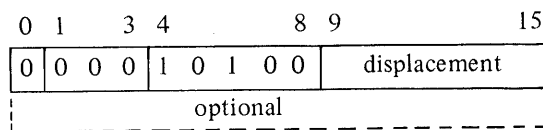
Branch on Indicator

Format:

```
0  1    3 4      8 9            15
┌─┬─┬─┬─┬─┬─┬─┬─┬─┬──────────────┐
│0│0 0 0│1 0 1 0 0│ displacement │
└─┴─────┴─────────┴──────────────┘
  optional
```

Description:

Branches to the specified location if either the greater than indicator (G) or the unlike signs indicator (U), but not both, is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BAGE

Instruction:

Branch if algebraically greater than or equal to

Type:

Branch on Indicator

Format:

```
0  1    3 4      8 9            15
┌─┬─┬─┬─┬─┬─┬─┬─┬─┬──────────────┐
│0│0 0 0│1 0 0 0 1│ displacement │
└─┴─────┴─────────┴──────────────┘
  optional
```

Description:

Branches to the specified location if either the less than indicator (L) or the unlike signs indica-tor (U), but not both, is equal to zero. If the J bit in the mode control (M) register is set, and if the

branch would have taken place, this instruction traps to trap vector #2.

BAL

Instruction:

Branch if algebraically less than

Type:

Branch on Indicator

Format:

```
0  1    3 4      8 9            15
┌─┬─┬─┬─┬─┬─┬─┬─┬─┬──────────────┐
│0│0 0 0│1 0 0 0 0│  displacement │
└─┴─────┴─────────┴──────────────┘
  optional
```

Description:

Branches to the specified location if either the less than indicator (L) or the unlike signs indica-tor (U), but not both, is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BALE

Instruction:

Branch if algebraically less than or equal to
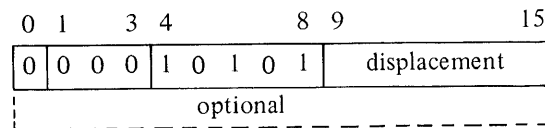
Type:

Branch on Indicator

Format:

```
0  1    3 4      8 9            15
┌─┬─┬─┬─┬─┬─┬─┬─┬─┬──────────────┐
│0│0 0 0│1 0 1 0 1│  displacement │
└─┴─────┴─────────┴──────────────┘
  optional
```

Description:

Branches to the specified location if either the greater than indicator (G) or the unlike sign indicator (U), but not both, is equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BBF

Instruction:

Branch if bit-test indicator false

Type:

Branch on Indicator

Format:

```
0  1     3  4        8  9              15
  0 0 0 0  0 1 0 1 1     displacement
          optional
```
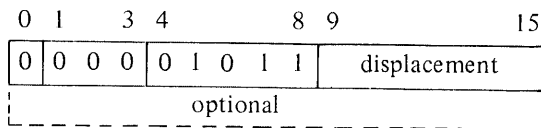
Description:

Branches to the specified location if the bit test indicator (B) is equal to zero. If the J list in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BBT

Instruction:

Branch if bit-test indicator true

Type:

Branch on Indicator

Format:

```
0  1     3  4        8  9              15
  0 0 0 0  0 1 0 1 0     displacement
          optional
```
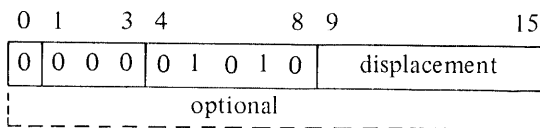
Description:

Branches to the specified location if the bit test indicator (B) is equal to one. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BCF

Instruction:

Branch if no carry

Type:

Branch on Indicator

Format:

```
0  1     3  4        8  9              15
  0 0 0 0  0 1 1 0 1     displacement
          optional
```
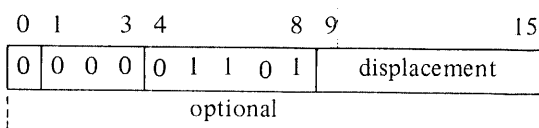
Description:

Branches to the specified location if the carry indicator (C) is equal to zero. If the J bit in the mode control (M) register is set, and if the branch

would have taken place, this instruction traps to trap vector #2.

BCT

Instruction:

Branch if carry

Type:

Branch on Indicator

Format:

```
0  1     3  4        8  9              15
  0 0 0 0  0 1 1 0 0     displacement
          optional
```
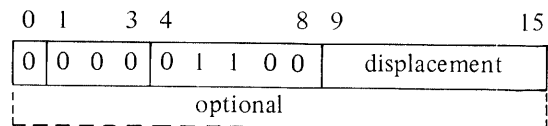
Description:

Branches to the specified location if the carry indicator (C) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BDEC

Instruction:

Branch and decrement

Type:

Branch on Register

Format:

```
0  1     3  4        8  9              15
  0   Rn    0 1 1 1 0     displacement
          optional
```
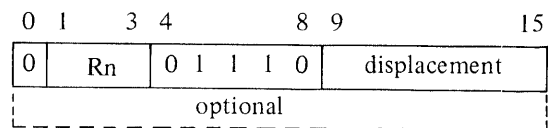
Description:

Subtracts one from the contents of the designated R-register and then branches to the specified location if the result is not equal to -1 (i.e., branches unless the register initially contained zero). If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BE

Instruction:

Branch if equal

Type:

Branch on Indicator

Format:

```
  0 1     3 4         8 9           15
 ┌─┬─────┬─────────┬────────────────┐
 │0│0 0 0│1 0 0 1 0│  displacement  │
 ├─┴─────┴─────────┴────────────────┤
 ┊            optional              ┊
 └──────────────────────────────────┘
```
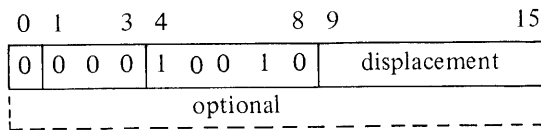
Description:

Branches to the specified location if neither the greater than indicator (G) nor the less than indicator (L) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BEVN

Instruction:

Branch if R-register even

Type:

Branch on Register
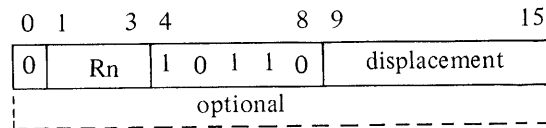
Format:

```
  0 1     3 4         8 9           15
 ┌─┬─────┬─────────┬────────────────┐
 │0│ Rn  │1 0 1 1 0│  displacement  │
 ├─┴─────┴─────────┴────────────────┤
 ┊            optional              ┊
 └──────────────────────────────────┘
```

Description:

Branches to the specified location if bit fifteen of the designated R-register is equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BEZ

Instruction:

Branch if R-register equal to 0

Type:

Branch on Register
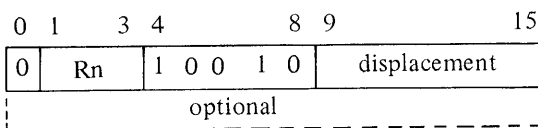
Format:

```
  0 1     3 4         8 9           15
 ┌─┬─────┬─────────┬────────────────┐
 │0│ Rn  │1 0 0 1 0│  displacement  │
 ├─┴─────┴─────────┴────────────────┤
 ┊            optional              ┊
 └──────────────────────────────────┘
```

Description:

Branches to the specified location if the contents of the designated R-register are equal to zero. If the J bit in the mode control (M) register

is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BG

Instruction:

Branch if greater than

Type:

Branch on Indicator

Format:

```
  0 1     3 4         8 9           15
 ┌─┬─────┬─────────┬────────────────┐
 │0│0 0 0│0 0 1 1 0│  displacement  │
 ├─┴─────┴─────────┴────────────────┤
 ┊            optional              ┊
 └──────────────────────────────────┘
```
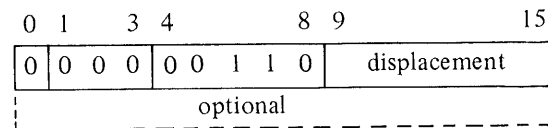
Description:

Branches to the specified location if greater than indicator (G) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BGE

Instruction:

Branch if greater than or equal to

Type:

Branch on Indicator

Format:

```
  0 1     3 4         8 9           15
 ┌─┬─────┬─────────┬────────────────┐
 │0│0 0 0│0 0 1 0 1│  displacement  │
 ├─┴─────┴─────────┴────────────────┤
 ┊            optional              ┊
 └──────────────────────────────────┘
```
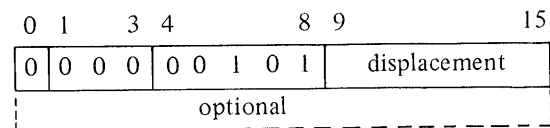
Description:

Branches to the specified location if the less than indicator (L) is equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BGEZ

Instruction:

Branch if R-register equal to or greater than 0

Type:

Branch on Register

Format:

```
 0  1    3 4      8 9          15
┌──┬─────┬─────────┬──────────────┐
│0 │ Rn  │1 0 0 1 │ displacement │
├──┴─────┴─────────┴──────────────┤
│            optional             │
└─────────────────────────────────┘
```
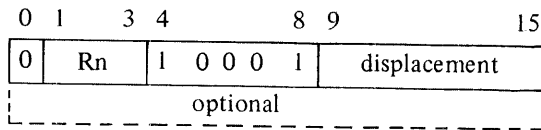
Description:

Branches to the specified location if bit zero of the designated R-registration is a zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BGZ

Instruction:

Branch if R-register greater than 0

Type:
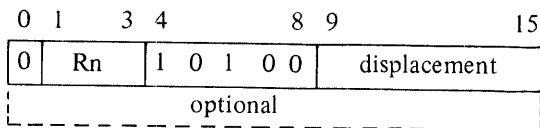
Branch on Register

Format:

```
 0  1    3 4       8 9          15
┌──┬─────┬──────────┬──────────────┐
│0 │ Rn  │1 0 1 0 0 │ displacement │
├──┴─────┴──────────┴──────────────┤
│             optional             │
└──────────────────────────────────┘
```

Description:

Branches to the specified location if bit zero of the designated R-register is equal to zero and if bits one to fifteen are not equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BINC

Instruction:

Branch and increment

Type:

Branch on Register

Format:

```
 0  1    3 4       8 9          15
┌──┬─────┬──────────┬──────────────┐
│0 │ Rn  │0 1 1 1 1 │ displacement │
├──┴─────┴──────────┴──────────────┤
│             optional             │
└──────────────────────────────────┘
```
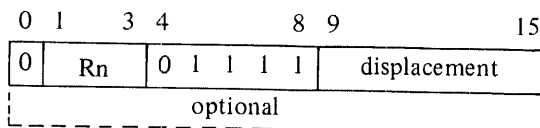
Description:

Adds one to the contents of the designated R-register and then branches to the specified

location if the result is not equal to zero (i.e., branches unless the register initially contains -1). If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BIOF

Instruction:

Branch if I/O indicator false

Type:

Branch on Indicator

Format:

```
 0  1    3 4         8 9          15
┌──┬───────┬──────────┬──────────────┐
│0 │0 0 0  │0 1 1 1 1 │ displacement │
├──┴───────┴──────────┴──────────────┤
│              optional              │
└────────────────────────────────────┘
```
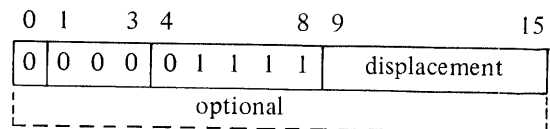
Description:

Branches to the specified location if the I/O indicator (I) is equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BIOT

Instruction:

Branch if I/O indicator true

Type:

Branch on Indicator

Format:

```
 0  1    3 4         8 9          15
┌──┬───────┬──────────┬──────────────┐
│0 │0 0 0  │0 1 1 1 0 │ displacement │
├──┴───────┴──────────┴──────────────┤
│              optional              │
└────────────────────────────────────┘
```
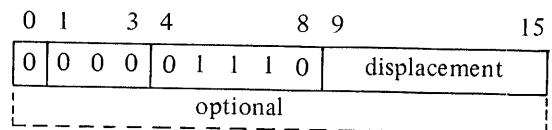
Description:

Branches to the specified location if the I/O indicator (I) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BL

Instruction:

Branch if less than

Type:

Branch on Indicator
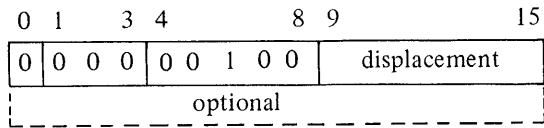
Format:

```
0  1    3  4        8  9              15
0| 0  0  0| 0  0  1  0  0| displacement |
         optional
```

Description:

Branches to the specified location if the less than indicator (L) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BLE

Instruction:
Branch if less than or equal to

Type:
Branch on Indicator

Format:

```
0  1    3  4        8  9              15
0| 0  0  0| 0  0  1  1  1| displacement |
         optional
```
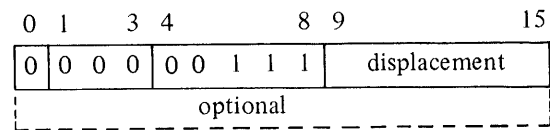
Description:

Branches to the specified location if the greater than indicator (G) is equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BLEZ

Instruction:
Branch if R-register equal to or less than 0

Type:
Branch on Register
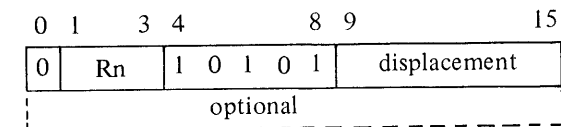
Format:

```
0  1    3  4        8  9              15
0| Rn | 1  0  1  0  1| displacement |
         optional
```

Description:

Branches to the specified location if bit zero of the designated R-register is equal to one, or if the contents are equal to zero. If the J bit in the mode content (M) register is set, and if the branch

would have taken place, this instruction traps to trap vector #2.

BLZ

Instruction:
Branch if R-register less than 0

Type:
Branch on Register
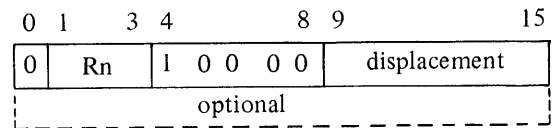
Format:

```
0  1    3  4        8  9              15
0| Rn | 1  0  0  0  0| displacement |
         optional
```

Description:

Branches to the specified location if bit zero of the designated R-register is a one. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BNE

Instruction:
Branch if not equal

Type:
Branch on Indicator
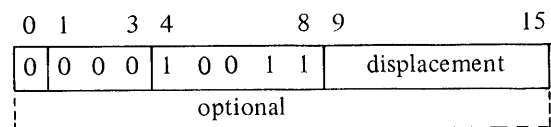
Format:

```
0  1    3  4        8  9              15
0| 0  0  0| 1  0  0  1  1| displacement |
         optional
```

Description:

Branches to the specified location if either the greater than indicator (G) or the less than indicator (L) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BNEZ

Instruction:
Branch if R-register not equal to 0

Type:
Branch on Register
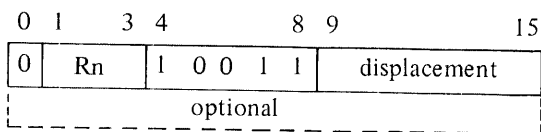
Format:

```
0  1    3 4       8 9          15
┌─┬─────┬────────┬──────────────┐
│0│ Rn  │1 0 0 1 1│ displacement │
└─┴─────┴────────┴──────────────┘
┊          optional              ┊
└────────────────────────────────┘
```

Description:

Branches to the specified location if the contents of the designated R-register are not equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BNOV

Instruction:
Branch if no R-register overflow

Type:
Branch on Indicator

Format:

```
0  1    3 4        8 9         15
┌─┬─────┬──────────┬────────────┐
│0│0 0 0│0 1 0 0 1 │displacement│
└─┴─────┴──────────┴────────────┘
┊          optional             ┊
└───────────────────────────────┘
```
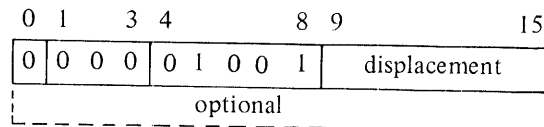
Description:

Branches to the specified location if the overflow indicator (OV) is equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BODD

Instruction:
Branch if R-register odd

Type:
Branch on Register
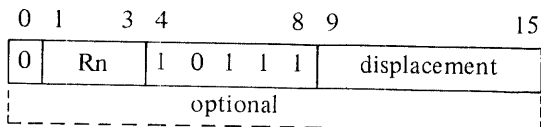
Format:

```
0  1    3 4        8 9         15
┌─┬─────┬──────────┬────────────┐
│0│ Rn  │1 0 1 1 1 │displacement│
└─┴─────┴──────────┴────────────┘
┊          optional             ┊
└───────────────────────────────┘
```

Description:

Branches to the specified location if bit fifteen of the designated R-register is equal to one. If the J bit in the mode control (M) register is set, and if

the branch would have taken place, this instruction traps to trap vector #2.

BOV

Instruction:
Branch if R-register overflow

Type:
Branch on Indicator

Format:

```
0  1    3 4        8 9         15
┌─┬─────┬──────────┬────────────┐
│0│0 0 0│0 1 0 0 0 │displacement│
└─┴─────┴──────────┴────────────┘
┊          optional             ┊
└───────────────────────────────┘
```
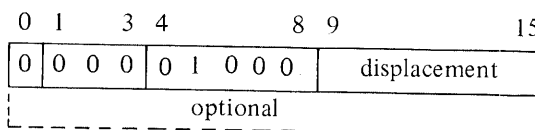
Description:

Branches to the specified location if the overflow indicator (OV) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BRK

Instruction:
Breakpoint

Type:
Generic

Format:

```
0                 7 8          15
┌─────────────────┬──────────────┐
│0 0 0 0 0 0 0 0  │0 0 0 0 0 1 0 │
└─────────────────┴──────────────┘
```
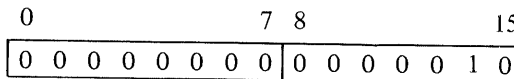
Description:

Causes a trap to trap vector 2; this instruction is used for debugging.

BSE

Instruction:
Branch if signs equal

Type:
Branch on Indicator

Format:

```
0  1    3 4        8 9         15
┌─┬─────┬──────────┬────────────┐
│0│0 0 0│1 0 1 1 1 │displacement│
└─┴─────┴──────────┴────────────┘
┊          optional             ┊
└───────────────────────────────┘
```
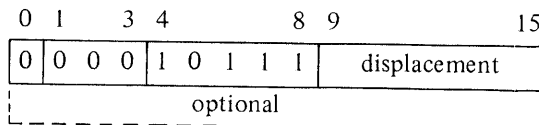
Description:
Branches to the specified location if the unlike signs indicator (U) is equal to zero. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

BSU

Instruction:
Branch if signs unlike

Type:
Branch on Indicator

Format:

0	1		3	4				8	9			15
0	0	0	0	1	0	1	1	0	displacement			
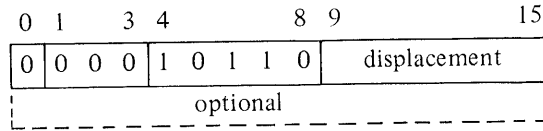
optional

Description:
Branches to the specified location if unlike signs indicator (U) is set. If the J bit in the mode control (M) register is set, and if the branch would have taken place, this instruction traps to trap vector #2.

CAD

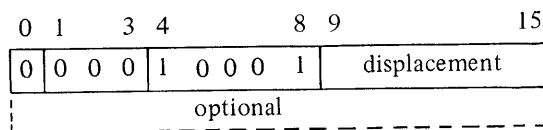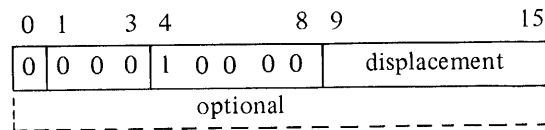**Instruction:**
Add carry bit to contents

Type:
Single Operands

Format:

0	1		3	4				8	9			15
1	0	0	0	1	1	1	0	1	address syllable			
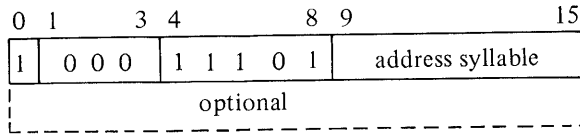
optional

Description:
Adds the contents of the C-bit in the I-register to the contents of the location specified in the address syllable.

The address syllable can specify a memory location, an immediate operand, or one of the R-registers.

The contents of the I-register are affected as follows:

- If a carry occurs during the operation, the C-bit is set to 1; otherwise, it is set to 0.

- If the result is more than 16 bits long, the OV-bit is set to 1; otherwise, it is set to 0. This cannot cause an overflow trap.

CL

Instruction:
Clear

Type:
Single Operand

Format:

0	1		3	4				8	9			15
1	0	0	0	0	1	1	1	0	address syllable			
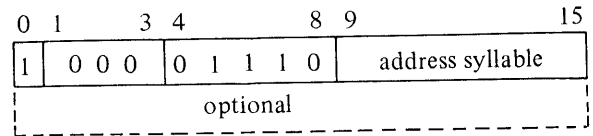
optional

Description:
Stores zeros in the location specified in the address syllable.

The address syllable can specify a memory location, an immediate operand, or one of the R-registers.

CLH

Instruction:
Clear halfword

Type:
Single Operand

Format:

0	1		3	4				8	9			15
1	0	0	0	0	1	1	1	1	address syllable			
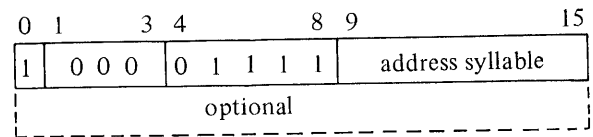
optional

Description:
Stores 0's in the halfword location specified in the address syllable.

The address syllable can specify a memory location, an immediate operand, or another R-register, with the byte being positioned as follows:

— memory location, not indexed	— left byte
— memory location, indexed	
index value even	— left byte
index value odd	— right byte
— immediate operand	— left byte
— R-register	— right byte

CMH

Instruction:
Compare halfword (byte) to R-register

Type:
Double Operand

Format:

```
0  1      3  4        8  9              15
┌──┬────────┬──────────┬──────────────────┐
│1 │  Rn    │0  0  0 1 1│ address syllable │
├──┴────────┴──────────┴──────────────────┤
│              optional                    │
└──────────────────────────────────────────┘
```
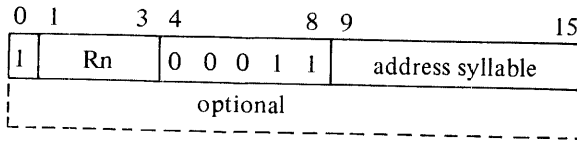
Description:
Compares the word in the designated R-register with the byte (sign extended) in the effective address and sets the G, L, and U indicators according to the results of the comparison. The address syllable can specify a memory location, an immediate operand, or another R-register, with the byte being positioned as follows:

— memory location, not indexed	— left byte
— memory location, indexed	
index value even	— left byte
index value odd	— right byte
— immediate operand	— left byte
— R-register	— right byte

The greater than (G) and less than (L) indicators are set or reset depending on the 16-bit unsigned contents of the two operands. The unlike sign (U) indicator is set if bit zero of both operands are the same, reset if different.

Example: R-register contains $(00FF)_{16}$
Effective address contains $(FF)_{16}$
CMR will set L and U, reset G

CMB

Instruction:
Compare contents to B-register

Type:
Double Operand
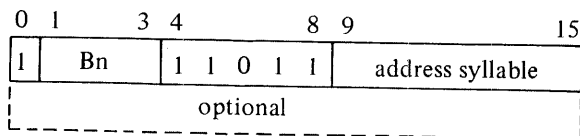
Format:

```
0  1      3  4        8  9              15
┌──┬────────┬──────────┬──────────────────┐
│1 │  Bn    │1  1  0 1 1│ address syllable │
├──┴────────┴──────────┴──────────────────┤
│              optional                    │
└──────────────────────────────────────────┘
```

Description:
Compares the word in the designated B-register with the word in the effective address and sets the G and L indicators according to the results of the comparison. The address syllable can specify a memory location, an immediate operand, or another B-register.

The greater than (G) and less than (L) indicators are set or reset depending on the 16-bit unsigned contents of the two operands. The setting of the unlike sign (U) indicator is not defined.

CMN

Instruction:
Compare address to null

Type:
Single Operand

Format:

```
0  1      3  4        8  9              15
┌──┬────────┬──────────┬──────────────────┐
│1 │0  0  0 │1  1  0 1 1│ address syllable │
├──┴────────┴──────────┴──────────────────┤
│              optional                    │
└──────────────────────────────────────────┘
```
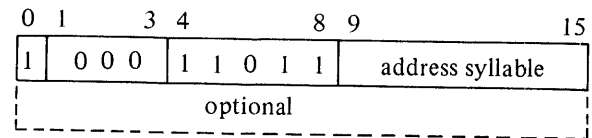
Description:
Compares the contents of the location or B-register specified by the address syllable to a null address (the address 0).

The contents of the I-register are affected as follows:

● The G-bit is set to 0 if the specified address is equal to null; otherwise, it is set to 1.
● The L-bit is set to 0.
● The U-bit is affected, but its value is undefined.

The address syllable can specify a memory location, an immediate operand, or one of the B-registers.

CMR

Instruction:
Compare to R-register

Type:
Double Operand
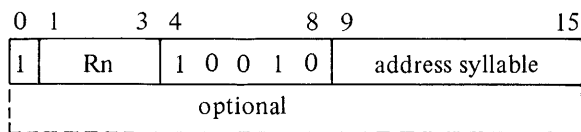
Format:

```
0  1      3 4        8 9              15
┌─┬──────┬──────────┬─────────────────┐
│1│  Rn  │1 0 0 1 0 │ address syllable │
├─┴──────┴──────────┴─────────────────┤
│              optional                │
└──────────────────────────────────────┘
```

Description:

Compares the word in the designated R-register with the word in the effective address and sets the G, L, and U indicators according to the results of the comparison. The address syllable can specify a memory location, an immediate operand, or another R-register.

The greater than (G) and less than (L) indicators are set or reset depending on the 16-bit unsigned contents of the two operands. The unlike sign (U) indicator is set if bit zero of both operands are the same, reset if different.

Note that this instruction can be used to do either a logical (alphabetical) comparison or an algebraic comparison. The branch instruction that follows will perform either an algebraic test or a logical test.

Example: R-register contains $(FFFF)_{16}$
Effective address contains $(7777)_{16}$
CMR will set G and U, reset L
BG (Branch if greater) will branch.
BAG (Branch if algebraically greater) will not.

CMV

Instruction:
Compare value to R-register

Type:
Short Value Immediate

Format:

```
0  1      3 4      7 8        15
┌─┬──────┬────────┬────────────┐
│0│  Rn  │1 1 0 1 │   value     │
└─┴──────┴────────┴────────────┘
```
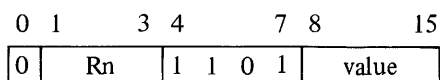
Description:

Compares the word in the designated R-register with the byte (with its sign extended) contained in the value field of the instruction and sets/resets the G (greater than), L (less than), and U (unlike signs) indicators according to the results of the comparison.

Some examples:

Contents of R-register	Value Field in Instruction	G	L	U
$(00AB)_{16}$	$(AB)_{16}$	0	1	1
$(FFAB)_{16}$	$(AB)_{16}$	0	0	0
$(FFAB)_{16}$	$(AA)_{16}$	1	0	0
$(-7)_{10}$	$(-7)_{10}$	0	0	0
$(-7)_{10}$	$(+7)_{10}$	1	0	1

CMZ

Instruction:
Compare to 0

Type:
Single Operand

Format:

```
0  1    3 4          8 9            15
┌─┬─────┬────────────┬───────────────┐
│1│0 0 0│1 0 0 1 1   │ address syllable│
├─┴─────┴────────────┴───────────────┤
│              optional               │
└──────────────────────────────────────┘
```
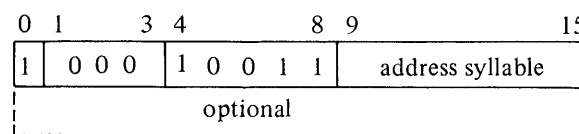
Description:

Compares the contents of the location specified in the address syllable to 0.

The address syllable can specify a memory location, an immediate operand, or one of the R-registers.

The contents of the I-register are affected as follows:

- If the contents of the specified location do not equal 0, the G-bit is set to 1; otherwise, it is set to 0.
- The L-bit is set to 0.
- If the first bit of the specified location equals 1, the U-bit is set to 1; otherwise, it is set to 0.

This instruction can be used to determine the size of the actual memory in a system. If non-installed memory is addressed, it will cause a trap through trap vector #15. This will also happen if indexing causes addresses of less than zero or greater than 64K to be generated.

CPL

Instruction:
Complement

Type:
Single Operand

Format:

```
0  1    3 4          8 9            15
┌─┬─────┬────────────┬───────────────┐
│1│0 0 0│0 1 1 0 0   │ address syllable│
├─┴─────┴────────────┴───────────────┤
│              optional               │
└──────────────────────────────────────┘
```
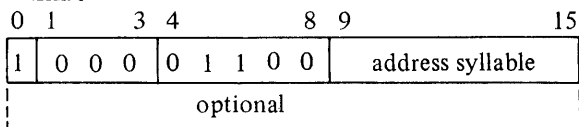
Description:
One's complements the contents of the location specified in the address syllable.

No indicators are affected. The address syllable can specify a memory location, an immediate operand, or one of the R-registers.

DAL

Instruction
Double-shift arithmetic-left

Type:
Shift Long
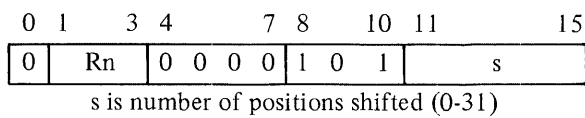
Format:

0	1 3	4 7	8 10	11 15
0	Rn	0 0 0 0	1 0 1	s

s is number of positions shifted (0-31)

Description:
Shifts the contents of the even-odd R-register pair (i.e., R2 and R3, R4 and R5, R6 and R7) identified in the Rn field (which must be odd) left the number of bit positions specified by the s field. The bit positions vacated by the shift are filled with binary 0's.

If the s field contains 0's, the shift distance is obtained from bits 11 through 15 of general register R1.

The contents of the I-register are affected as follows:

- If the contents of bit 0 in the even-numbered R-register changes, the OV-bit is set to 1: otherwise, it is set to 0.
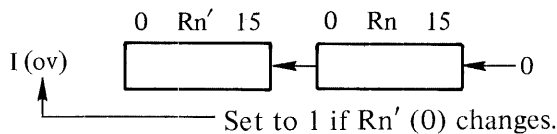
Pictorial Representation

I (ov)   0 Rn′ 15   0 Rn 15   ←—0
Set to 1 if Rn′ (0) changes.

DAR

Instruction:
Double-shift arithmetic-right

Type:
Shift Long

Format:

0	1 3	4 7	8 10	11 15
0	Rn	0 0 0 0	1 1 1	s

s is number of positions shifted (0-31)
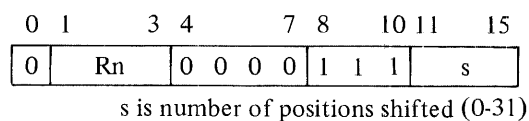
Description:
Shifts the contents of the even-odd R-register pair (i.e., R2 and R3, R4 and R5, R6 and R7) identified in the Rn field (which must be odd) right the number of bit positions specified by the s field. The bit positions vacated by the shift are filled with the sign value originally contained in bit 0.

If the s field contains 0's, the shift distance is obtained from bits 11 through 15 of general register R1.

The contents of the I-register are affected as follows:

- C-bit contains the last binary digit shifted out of the odd-numbered R-register.

Pictorial Representation:

Rn′(0)...   0 Rn′ 15   0 Rn 15   ►— I(c)
Saves last bit shifted out of Rn(15)

DCL

Instruction:
Double-shift closed-left

Type:
Shift Short

Format:

0	1 3	4 7	8 11	12 15
0	Rn	0 0 0 0	0 0 1 1	s

s is number of positions shifted (0-15)
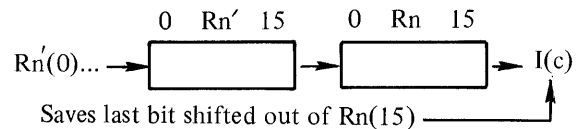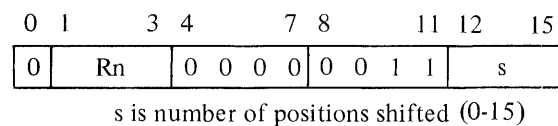
Description:
Shifts the contents of the even-odd R-register pair (i.e., R2 and R3, R4 and R5, R6 and R7) identified in the Rn field (which must be odd) left the number of bit positions specified by the s field. The bits shifted out of the even-numbered R-register are placed in the bit positions of the odd-numbered R-register vacated as the bits are shifting left.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

Pictorial Representation:

0 Rn′ 15   0 Rn 15

DCR

Instruction:
Double-shift closed-right
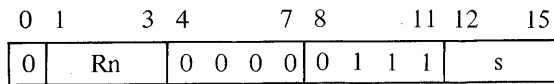
Type:
Shift Short

Format:

0	1		3	4			7	8			11	12			15
0	Rn			0	0	0	0	0	1	1	1	s			

s is number of positions shifted (0-15)

Description:
Shifts the contents of the even-odd R-register pair (i.e., R2 and R3, and R4 and R5, R6 and R7) identified in the Rn field (which must be odd) right the number of bit positions specified by the s field. The bits shifted out of the odd-numbered R-register are placed in the bit positions of the even-numbered R-register vacated as the bits are shifting right.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

Pictorial Representation:
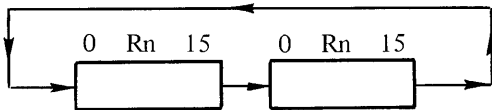
DEC

Instruction:
Decrement

Type:
Single Operand

Format:

0	1		3	4			8	9		15
1	0 0 0			1	0	0	1	address syllable		
	optional									
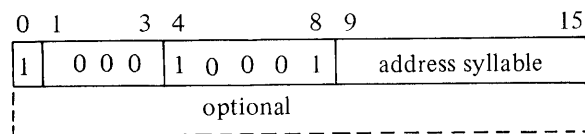
Description:
Decrements by 1 the contents of the location or register specified in the address syllable, then copies bit 0 of the addressed word or register into I(b).

This instruction operates in read modify write (RMW) mode, which prevents any other processor in a multiprocessor environment from accessing the location being modified until the modification is completed.

The address syllable can specify a memory location, an immediate operand, or one of the R-registers.

The contents of the I-register are affected as follows:

- If the decrementation causes a carry to occur, the C-bit is set to 1; otherwise, it is set to 0.
- If the value being decremented was -32768 (-2^{15}), I(OV) is set to 1; otherwise, I(OV) is cleared to 0. However, this can never cause an overflow trap.
- I(b) is set as described above.

DIV

Instruction:
Divide R-register

Type:
Double Operand

Format:

0	1		3	4				8	9	15
1	Rn			0	0	1	1	0	address syllable	
	optional									
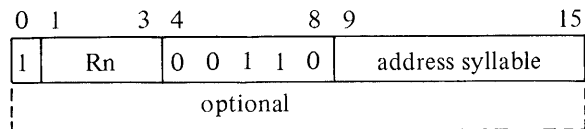
Description:
If the designated R-register is R1 to R6, its contents are divided by the word at the effective address and the remainder is lost; if the designated R-register is R7, the double precision value in R6 and R7 is divided by the word at the effective address with the quotient being developed in R7 and the remainder in R6. The address syllable can specify a memory location, an immediate operand, or another R-register.

The contents of the I-register are affected as follows:

1. I(OV) is set to 1 if
   a. The divisor = 0
   b. The dividend is -2^{15} times the divisor.
   c. The quotient is greater than $2^{15} -1$ or less than -2^{15}.
   Otherwise I(OV) is cleared to 0.
   Divide operations that cause I(OV) to be set terminate with all operands unchanged.

2. The carry indicator, I(C), is set only if the remainder is not 0 *and* if the remainder is not stored in R6 (i.e. when the first operand does not specify R7). If R7 were specified as the first operand, the remainder would be stored in R6 and the carry bit would be unchanged whether or not the remainder was zero.

DOL

Instruction:
Double-shift open-left

Type:
Shift Long
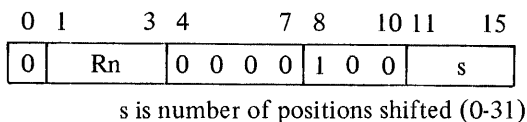
Format:

0	1	3	4	7	8	10	11	15
0	Rn		0 0 0 0		1 0 0		s	

s is number of positions shifted (0-31)

Description:
Shifts the contents of the even-odd R-register pair (i.e., R2 and R3, R4 and R5, R6 and R7) identified in the Rn field (which must be odd) left the number of bit positions specified by the s field. The bit positions vacated by the shift are filled with binary 0's.

If the s field contains 0's, the shift distance is obtained from bits 11 through 15 of general register R1.

The contents of the I-register are affected as follows:

● C-bit contains the last binary digit shifted out of the even-numbered R-register.

Pictorial Representation:

Saves last bit shifted out of Rn'(0)
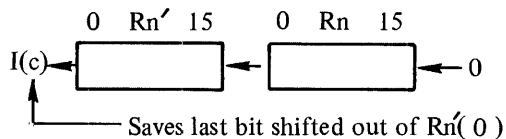
DOR

Instruction:
Double-Shift open-right

Type:
Shift Long
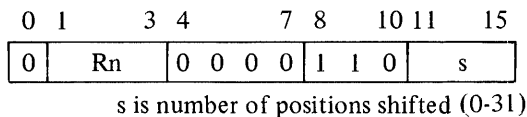
Format:

0	1	3	4	7	8	10	11	15
0	Rn		0 0 0 0		1 1 0		s	

s is number of positions shifted (0-31)

Description:
Shifts the contents of the even-odd R-register pair (i.e., R2 and R3, R4 and R5, R6 and R7) identified in the Rn field (which must be odd) right the number of bit positions specified by the s field. The bit positions vacated by the shift are filled with binary 0's.

If the s field contains 0's the shift distance is obtained from bits 12 through 15 of general register R1.

The contents of the I-register are affected as follows:

● C-bit contains the last binary digit shifted out of the odd-numbered R-register.

Pictorial Representation:

Saves last bit shifted out of Rn(15)
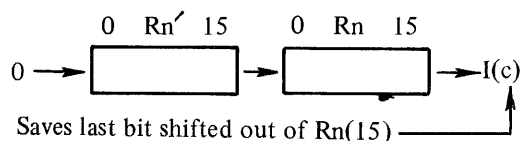
ENT

Instruction:
Enter

Type:
Single Operand

Format:

0	1	3	4	8	9	15
1	0 0 0		1 0 1 1 1		address syllable	
optional						
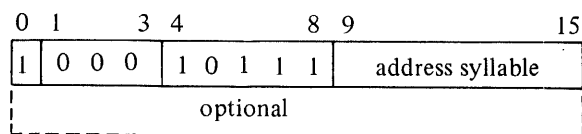
Description:
Puts the processor into the unprivileged (user) mode and then jumps to the location specified by the effective address. If the J-bit in the mode-control (M) register is on, this instruction traps to trap #2.

No indicators are affected. The address syllable must specify a memory location, not a register or an immediate operand.

HLT

Instruction:
Halt

Type:
Generic

Format:

```
0                   7 8              15
| 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 |
```
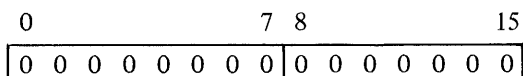
Description:

Stops program execution. HLT state is indicated on the control panel. All interrupts will be honored.

The P-bit in the S-register must be set to 1 (i.e., the central processor must be in the privileged state) for this instruction to be executed. If not, the unprivileged use of a privileged operation is signified by a trap to trap vector #13.

INC

Instruction:
Increment

Type:
Single Operand

Format:

```
0 1     3 4       8 9             15
|1| 0 0 0 | 1 0 1 0 1 | address syllable |
|          optional                      |
```
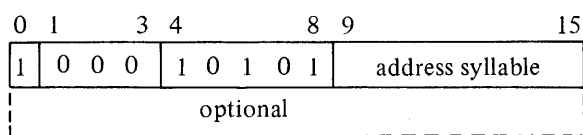
Description:

Copies bit 0 of the contents of the location or register specified in the address syllable into I(b), then increments by 1 the contents of the location or register.

This instruction operates in read modify write (RMW) mode, which prevents any other processor in a multiprocessor environment from accessing the location being modified until the modification is completed.

The address syllable can specify a memory location, an immediate operand, or another R-register.

The contents of the I-register are affected as follows:

- If the incrementation causes a carry to occur, the C-bit is set to 1; otherwise, it is set to 0.
- If the value being incremented was 32767, I(OV) is set to 1; otherwise it is cleared to 0. However, this can never cause an overflow trap.

IO

Instruction:
Input Output (word)

Type:
Input/Output

Formats:

```
0 1   3 4       8 9                    15
|1| 0 0 0 | 0 0 0 0 0 | data address syllable |
|                 optional                    |
| channel         |      function             |
```

or

```
0 1   3 4       8 9                    15
|1| 0 0 0 | 0 0 0 0 0 | data address syllable |
|                 optional                    |
| 0 0 0 0 0 0 x x x | channel address syllable |
|                 optional                     |
```
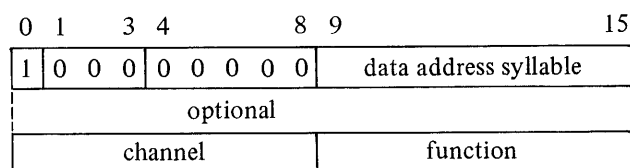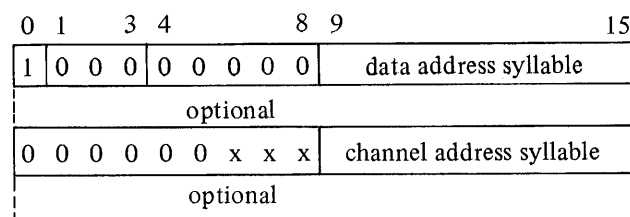
Description:

This is a privileged instruction that can be executed only if the P-bit in the status register is set to one; otherwise the instruction traps through trap vector #13.

This instruction initiates an I/O command bus cycle that either outputs a word to a channel or requests the input of a word from a channel. If the channel accepts the I/O command, the input/output (I) indicator is set to a one; if it does not accept the command, the I-bit is reset to zero.

The location of the word to be output or of where the word is to be input is described by the data address syllable in the instruction. This address syllable is identical to those in single – and double-operand instructions and can specify a memory location, an immediate operand, or a R-register. If a memory location is specified on an output, for example, the data word is first read from the memory to the CPU and then output from the CPU to the channel. The memory does

not send or receive the data directly to or from the channel.

The channel number is a ten-bit value contained in the same word with a six-bit function code. This word is contained directly in the instruction, or, if the channel number field (bit 0-5) in the instruction is zero, in a location pointed to by the channel address syllable.[1] If the latter is utilized, it is of the general address syllable form and can specify a memory location or a R-register.

The channel number can specify an output channel (if it is odd) or an input channel (if it is even). This has nothing to do with whether the I/O instruction initiates an output command or an input command. (It is possible to output to input channels or input from output channels, as well as output to output and input from input.)

The direction of the command is determined by the function code, which also specifies the type of data to be input or output. The function code normally addresses a set-up, control or status register in the channel. However, it could specify a data buffer and thus be used to implement a programmed input/output operation. (The latter technique is not used by standard I/O channels which all work on a DMA basis of I/O.)

Function codes are thus dependent on the design of a particular channel controller. However, the following codes have been assigned and are used by standard channels:

Input codes:
    02 — Input interrupt control word
    06 — Input task word
    0C — Input range
    10 — Input configuration word A
    12 — Input configuration word B
    18 — Input status word #1
    1A — Input status word #2
    26 — Input device I.D.
Output codes:
    01 — Output control word
    03 — Output interrupt control word
    07 — Output task
    09 — Output address (see note)
    0D — Output range (see note)
    11 — Output configuration word A
    13 — Output configuration word B

---

[1]On processor to processor transfers, a CAS must be used as the first six bits of a processor channel number are always zero.

NOTE: The IO instruction should not use codes 09 and 0D as the address and range should be output with an IOLD instruction.

IOH

Instruction:
    Input/output half-word

Type:
    Input/Output

Formats:

```
0 1     3 4         8 9               15
+-+-----+---------+---------------------+
|1|0 0 0|0 0 0 1 0| data address syllable|
+-+-----+---------+---------------------+
|              optional                  |
+-----------------+---------------------+
|     channel     |       function      |
+-----------------+---------------------+
```

or

```
0 1     3 4         8 9               15
+-+-----+---------+---------------------+
|1|0 0 0|0 0 0 1 0| data address syllable|
+-+-----+---------+---------------------+
|              optional                  |
+-----------------+---------------------+
|0 0 0 0 0 0 x x x| channel address syllable|
+-----------------+---------------------+
|              optional                  |
+----------------------------------------+
```

Description:
    This is a privileged instruction that is identical to the IO instruction (see previous page) except that it transfers a byte rather than a word. The data address syllable generates a 17-bit byte address, e.g., the right half of a register, the left half of an unindexed memory location, on either half of an indexed memory location depending on the index count. The contents of the other half of the word remain unchanged.

This instruction is designed for programmed I/O operations. It is not currently used by Honeywell implemented controllers.

IOLD

Instruction:
    Input/output load

Type:
    Input/Output

Formats:

0	1		3	4				8	9					15
1	0	0	0	0	0	0	1	1	buffer address syllable					

optional

channel	function (09)

x	x	x	x	x	x	x	x	x	range address syllable

optional

or

0	1		3	4				8	9					15
1	0	0	0	0	0	0	1	1	buffer address syllable					

optional

0	0	0	0	0	0	x	x	x	channel address syllable

optional

x	x	x	x	x	x	x	x	x	range address syllable

optional
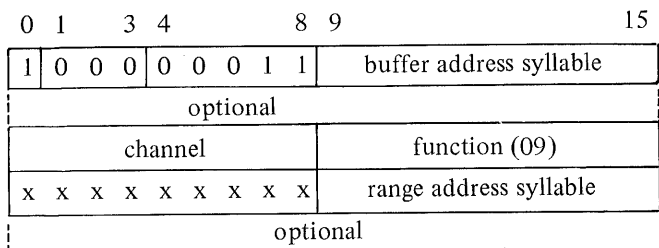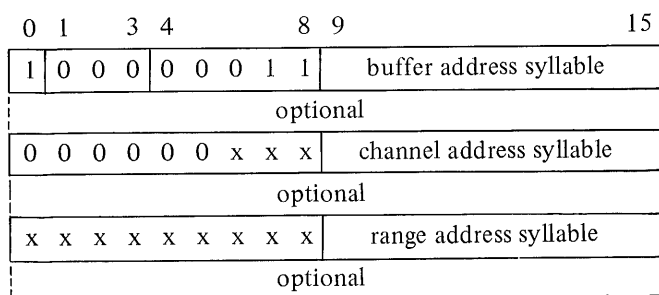
Description:

This is a privileged instruction that is used to set up a device for DMA operation by outputting an address and a range to it. It is similar in function to two consecutive IO instructions (see previous pages) in that it initiates two I/O output commands, one with a function code of $(09)_{16}$ and one with a function code of $(OD)_{16}$.

The main difference is that it outputs a 17-bit byte address to the DMA address register. The address register is 24 bits in length as opposed to the 16 bit length of the other registers in the channel. To generate a 17 bit word, the IOLD outputs the effective address of the buffer as specified by the "buffer" address syllable, not the contents of the location pointed to by it.

This address is split when put on the bus, with the 16 least significant bits being put on the data-lines and the high-order bits in the "module" field of the address bus (see below).

The "buffer" address syllable must define a memory location. If it is not indexed the effective address will define the left byte in a word; if it is indexed it can specify either side.

The channel can either be defined within the instruction or can be pointed to by the channel address syllable. The function code must be $(09)_{16}$.

After the first output command, 04 is automatically added to the function code and another output command is initiated. This command

outputs the contents (a 16 bit word) of the location pointed to by the range address syllable. A memory location, immediate operand, or R register form of addressing may be used. The range itself is a signed 16-bit value which defines the number of bytes to be transferred.

The formats of the I/O output command bus cycles are as follows:

	0	7 8	17	23
Address bus	Module No.	Channel Number	Function=$(09)_{16}$	
Data bus		Byte address	within module	

	0		15

Address bus	Not used	Channel Number	Function=$(OD)_{16}$	
Data bus		Range ($\pm$32K)		
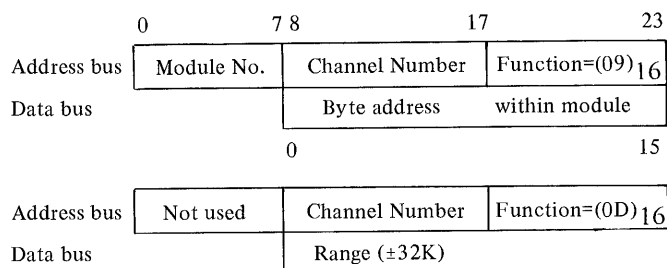
JMP

Instruction:
Jump

Type:
Single Operand

Format:

0	1		3	4				8	9					15
1	0	0	0	0	0	1	1	1	address syllable					

optional
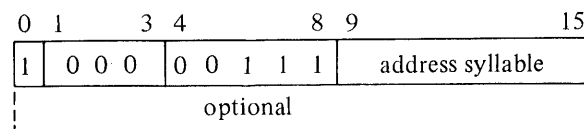
Description:

Jumps to the location specified in the address syllable, unless the J bit in the mode control (M) register is set, in which case it traps to trap vector #2.

No indicators are affected. The address syllable can specify a memory address, but not a register or an immediate operand.

LAB

Instruction:
Load effective address into B-register

Type:
Double Operand

Format:

0	1		3	4				8	9					15
1	Bn			1	0	1	1	1	address syllable					

optional
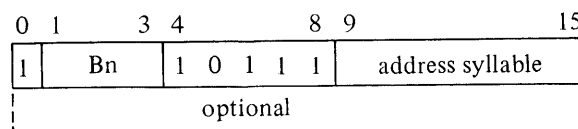
Description:

Loads the 16-bit effective address specified by the address syllable into the designated B-register. Note that this is the address itself, not its contents. No indicators are affected. The address syllable can specify a memory address or an immediate operand, but not a register.

Example: Assume the following:

Register R3 contains $(0007)_{16}$
Register B5 contains $(B010)_{16}$
Memory location $(B010)_{16}$ contains $(FA03)_6$

The instruction LAB $B7, *$B5.$R3 (indirect through B5 indexed by R3) will load B7 with $(FA0A)_{16}$.

LB

Instruction:

Load bit

Type:

Single Operand
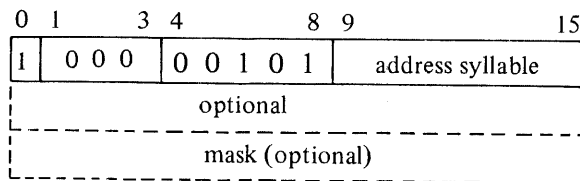
Format:

```
0  1      3 4        8 9              15
| 1 | 0 0 0 | 0 0 1 0 1 | address syllable |
|        optional               |
|        mask (optional)        |
```

Description:

This instruction is used to load the B-bit indicator in the I register with either a single bit or with the result of a test on a group of bits in a word. If any are on, the B bit will be set to 1; if none are on, to zero.

To address a single bit, the address syllable must specify an indexed memory address. The index value will count bits relative to bit zero of the effective address.

To test a group of bits in a word, a mask word following the instruction is utilized. Bit positions in the word at the effective address that correspond to one bits in the mask are tested. In this form the address syllable can specify a memory location (unindexed), an immediate operand, or another R-register.

For example, to test bit 13 in a word, indexed addressing with an index value of 13 should be used (or -3, +29, etc.). To test bits 13, 14, and 15, a mask with a value of 0007 should be used.

LBC

Instruction:

Load bit and complement

Type:

Single Operand
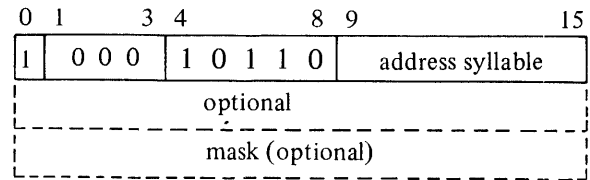
Format:

```
0  1      3 4        8 9              15
| 1 | 0 0 0 | 1 0 1 1 0 | address syllable |
|        optional               |
|        mask (optional)        |
```

Description:

This instruction is used to load the B-bit indicator in the I register with either a single bit or with the result of a test on a group of bits in a word. If any are on, the B bit will be set to 1; if none are on, to zero. The single bit loaded or the group of bits tested will then be complemented.

To address a single bit, the address syllable must specify an indexed memory address. The index value will count bits relative to bit zero of the effective address.

To test a group of bits in a word, a mask word following the instruction is utilized. Bit positions in the word at the effective address that correspond to one bits in the mask are tested. In this form the address syllable can specify a memory location (unindexed), an immediate operand, or another R-register.

This instruction operates in read modify write (RMW) mode, which prevents any other processor in a multiprocessor environment from accessing the location being modified until the modification is completed.

LBF

Instruction:

Load bit and set false

Type:

Single Operand
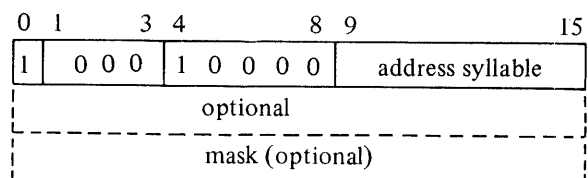
Format:

```
0  1      3 4        8 9              15
| 1 | 0 0 0 | 1 0 0 0 0 | address syllable |
|        optional               |
|        mask (optional)        |
```

Description:

This instruction is used to load the B-bit indicator in the I register with either a single bit or with the result of a test on a group of bits in a word. If any are on, the B bit will be set to 1; if none are on, to zero. The single bit loaded on the group of bits tested will then be set to zero(s).

To address a single bit, the address syllable must specify an indexed memory address. The index value will count bits relative to bit zero of the effective address.

To test a group of bits in a word, a mask word following the instruction is utilized. Bit positions in the word at the effective address that correspond to one bits in the mask are tested. In this form the address syllable can specify a memory location (unindexed), an immediate operand, or another R-register.

This instruction operates in read modify write (RMW) mode, which prevents any other processor in a multiprocessor environment from accessing the location being modified until the modification is completed.

LBS

Instruction:

Load bit and swap

Type:

Single Operand
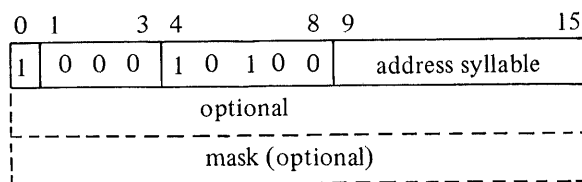
Format:

```
0 1      3 4       8 9              15
┌─┬───────┬─────────┬─────────────────┐
│1│ 0 0 0 │1 0 1 0 0│ address syllable │
├─┴───────┴─────────┴─────────────────┤
│              optional                │
└─────────────────────────────────────┘
│           mask (optional)            │
└─────────────────────────────────────┘
```

Description:

This instruction is used to load the B-bit indicator in the I register with either a single bit or with the result of a test on a group of bits in a word. If any are on, the B bit will be set to 1; if none are on, to zero. The single bit loaded on the group of bits tested will then be set to the previous contents of the B-bit.

To address a single bit, the address syllable must specify an indexed memory address. The index value will count bits relative to bit zero of the effective address.

To test a group of bits in a word, a mask word following the instruction is utilized. Bit positions in the word at the effective address that corre-

spond to one bits in the mask are tested. In this form the address syllable can specify a memory location (unindexed), an immediate operand, or another R-register.

This instruction operates in read modify write (RMW) mode, which prevents any other processor in a multiprocessor environment from accessing the location being modified until the modification is completed.

LBT

Instruction:

Load bit and set true

Type:

Single Operand
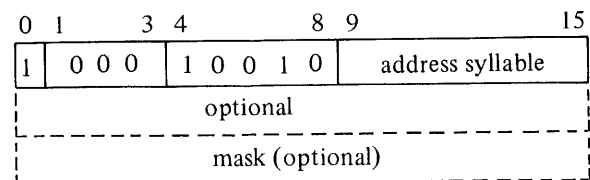
Format:

```
0 1      3 4       8 9              15
┌─┬───────┬─────────┬─────────────────┐
│1│ 0 0 0 │1 0 0 1 0│ address syllable │
├─┴───────┴─────────┴─────────────────┤
│              optional                │
└─────────────────────────────────────┘
│           mask (optional)            │
└─────────────────────────────────────┘
```

Description:

This instruction is used to load the B-bit indicator in the I register with either a single bit or with the result of a test on a group of bits in a word. If any are on, the B bit will be set to 1; if none are on, to zero. The single bit loaded or the group of bits tested will then be set to one.

To address a single bit, the address syllable must specify an indexed memory address. The index value will count bits relative to bit zero of the effective address.

To test a group of bits in a word, a mask word following the instruction is utilized. Bit positions in the word at the effective address that correspond to one bits in the mask are tested. In this form the address syllable can specify a memory location (unindexed), an immediate operand, or another R-register.

This instruction operates in read modify write (RMW) mode, which prevents any other processor in a multiprocessor environment from accessing the location being modified until the modification is completed.

LDB

Instruction:

Load B-register

Type:
Double Operand

Format:

```
0  1       3 4        8 9              15
| 1 |  Bn  | 1  1  0  0  1 | address syllable |
|        optional                            |
```
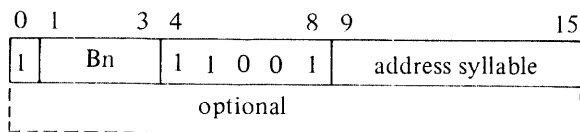
Description:
Loads the designated B-register with the word contained at the effective address. No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another B-register.

LDH

Instruction:
Load Half-word (byte) into R-register

Type:
Double Operand

Format:

```
0  1       3 4        8 9              15
| 1 |  Rn  | 0  0  0  0  1 | address syllable |
|        optional                            |
```

Description:
Loads the byte contained at the effective address into the right half of the designated R-register, with the sign being extended into the left half, bits 0-7. No indicators are affected.

The effective address can specify a memory location, an immediate operand, or another R-register, with the byte being positioned as follows:

— memory location, not indexed	— left byte
— memory location, indexed	
index value even	— left byte
index value odd	— right byte
— immediate operand	— left byte
— R-register	— right byte

Example: Assume that:
- memory location 1000 contains $(6789)_{16}$
- register R1 contains 0
- register R2 contains 1
- register B1 contains $(1000)_{16}$

then if LDH $R5, $B1.$R1 is executed: R5 will contain $(0067)_{16}$
but if LDH $R5, $B1.$R2 is executed: R5 will contain $(0089)_{16}$

LDI

Instruction:
Load double-word integer

Type:
Single Operand

Format:

```
0  1       3 4        8 9              15
| 1 | 0 0 0 | 1  1  0  0  1 | address syllable |
|        optional                            |
```
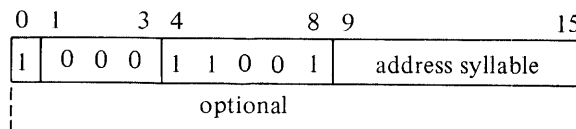
Description:
Loads the word contained at the effective address into R6 and the following word into R7. No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another R-register as follows:

- Memory location: The left-hand word of a double-word pair will be addressed. Auto-increment and auto-decrement modes of addressing will add (subtract) two from the base register. A value in the index register will count double words; it is shifted one place to the left before being applied. Auto-indexing will cause one to be added (subtracted) from the index register.
- Immediate operand: This will be a double-word operand and thus the instruction will be three words in length.
- Register operand: This form of addressing must address the right-hand register containing a double-word pair, i.e., either R3, which loads the contents of R2 and R3 into R6 and R7, or R5, which selects R4 and R5.

LDR

Instruction:
Load R-register

Type:
Double Operand

Format:

```
0  1       3 4        8 9              15
| 1 |  Rn  | 1  0  0  0  0 | address syllable |
|        optional                            |
```
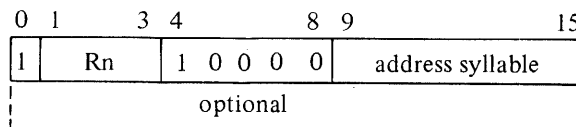
Description:

Loads the designated R-register with the word contained at the effective address. No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another R-register.

LDV

Instruction:
Load value

Type:
Short Value Immediate

Format:

| 0 | 1 | 3 | 4 | 7 | 8 | 15 |

| 0 | Rn | 1 1 0 0 | value |
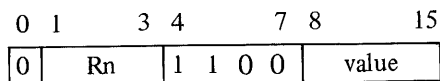
Description:

Loads the byte contained in the value field of the instruction into the right half of the designated R-register with the sign being extended into the left half. No indicators are affected.

LEV

Instruction:
Level Change

Type:
Single Operand

Format:

| 0 | 1 | 3 | 4 | 8 | 9 | 15 |

| 1 | 0 0 0 | 1 1 1 0 0 | address syllable |
| optional |
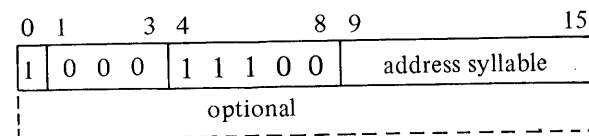
Description:

Sets or resets level activity bits according to the contents of the location indicated by the address syllable.

The following bit configurations in the indicated location produce the actions described below.

Schedule Interrupt Level, Scan and Dispatch
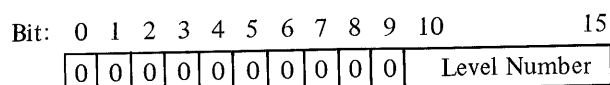
Bit: 0 1 2 3 4 5 6 7 8 9 10   15

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Level Number |

The level activity bit for the designated level will be set. The level activity bits will be scanned and the highest active level ascertained. The context of the current level will be saved (unless the current level is the highest active level). The context of the highest active level will be restored (again, unless the current level is the highest active level).

Schedule Interrupt Level, Defer Interrupt

Bit: 0 1 2 3 4 5 6 7 8 9 10   15

| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Level Number |
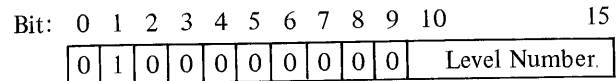
The level activity bit for the designated level will be set. Execution will continue at the current level.
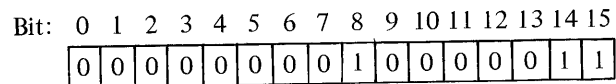
Inhibit

Bit: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

The level activity bit for priority level 3 will be set. The interrupt vector for priority level 3 will be set equal to the interrupt vector for the current level. Execution of the current task continues at priority level 3.

Schedule Interrupt Level, Suspend, Scan and Dispatch
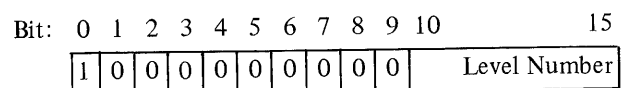
Bit: 0 1 2 3 4 5 6 7 8 9 10   15

| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Level Number |

The level activity bit for the designated level will be set. The level activity bit for the current level will be reset. The level activity bits will be scanned and the highest level ascertained. The context of the current level will be saved. The context of the highest active level will be restored.

Suspend, Inhibit
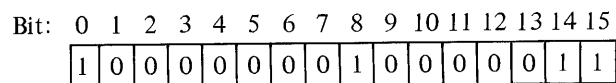
Bit: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

The level activity bit for the current level will be reset. The level activity bit for priority level 3 will be set. The interrupt vector for priority level 3 will be set equal to the interrupt vector for the current level. Execution of the task continues at priority level 3.

Enable

Bit: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

Enable is used to end execution at priority level 3. The level activity bit for priority level 63 will be set. The level activity bit for priority level 3 will be reset. The level activity bits will be scanned and the highest active level ascertained. The context of the current level is saved (unless the level where the inhibit originated is now the highest active level). The context of the highest active level will be restored (again, unless the level where the inhibit originated is now the highest active level).

The address syllable can specify a memory location, an individual operand, or an R-register.

The P-bit in the S-register must be set to 1 (i.e., the central processor must be in the privileged state) for this instruction to be executed. If the P-bit is not set to 1, the unprivileged use of a privileged operation is signified by a trap to trap vector #13.

The contents of the S-register are affected as follows:

- Bits 10 through 15 of the S-register will be set to indicate the priority level at which processing continues after execution of the LEV instruction.

LLH

Instruction:
Load logical half-word (byte) into R-register

Type:
Double Operand

Format:

0	1 3	4 8	9 15
1	Rn	0 0 1 0 1	address syllable
optional			

Description:
Loads the byte contained at the effective address into the right half of the designated R-register, with the left half, bits 0-7 being cleared to zero. No indicators are affected.

The effective address can specify a memory location, an immediate operand, or another R-register, with the byte being positioned as follows:

- memory location, not
  indexed   — left byte
- memory location, indexed
    index value even   — left byte
    index value odd   — right byte
- immediate operand   — left byte
- R-register   — right byte

Example: Assume that:

- memory location 1000 contains $(6789)_{16}$
- register R1 contains 0
- register R2 contains 1
- register B1 contains $(1000)_{16}$

then if LLH $R5, $B1.$R1 is executed: R5 will contain $(0067)_{16}$
but if LLH $R5, $B1.$R2 is executed: R5 will contain $(0089)_{16}$

LNJ

Instruction:
Load B-register and jump (Link Jump)

Type:
Double Operand

Format:

0 1	3 4	8 9	15
1	Bn	0 0 1 1 1	address syllable
optional			

Description:
Loads the address of the next sequential instruction into the designated B-register and jumps to the location specified by the effective address. If the J-bit in the M1-register is on, this instruction traps to trap #2.

No indicators are affected. The address syllable must specify a memory location, but not a register or an immediate operand.

MCL

Instruction:
Call monitor via trap

Type:
Generic

Format:

0	7 8	15
0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	

Description:
Calls monitor by a trap to trap vector 1.

MLV

Instruction:
Multiply by value

Type:
Short Value Immediate

Format:

```
 0  1      3  4      7  8        15
+--+------+--+--+--+--+----------+
|0 |  Rn  |1 |1 |1 |1 |  value   |
+--+------+--+--+--+--+----------+
```
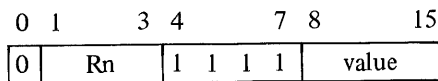
Description:
Multiplies the value in the designated R-register by the value (with sign extended) contained in the instruction. A single precision 16-bit product is formed, with overflow and carry bits set if necessary, unless the designated register is R7, in which case a double precision 32-bit signed product is developed in R6 and R7.

MTM

Instruction:
Modify or test M-register

Type:
Double Operand

Format:

```
 0  1      3  4        8  9              15
+--+------+--+--+--+--+--+----------------+
|1 |  M1  |0 |0 |0 |0 |0 | address syllable|
+--+------+--+--+--+--+--+----------------+
|              optional                   |
+- - - - - - - - - - - - - - - - - - - - -+
```
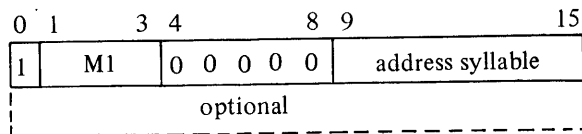
Description:
Modifies or tests the contents of the M-register identified in the first operand with the contents (mask) of the location specified by the address syllable.

The mask is treated as two 8-bit fields; then, depending on the content of corresponding bits in the two fields (i.e., bit 1 in the first field and bit 1 in the second; bit 2 in the first field and bit 2 in the second; etc.), the corresponding bit in the M-register (i.e., if bit 1 in the two mask fields,

then bit 1 in the M-register) is altered as described below:

- If bit n in the first mask field is 1, the corresponding bit in the M-register is loaded with the contents of the corresponding bit from the second mask field (i.e., M-register is modified).
- If bit n in the first mask field is 0 and the same bit in the second mask field is 1, the corresponding bit in the M-register is inclusively ORed with the contents of the B-bit in the I-register. If the result of the ORing is 1, the B-bit is set to 1; otherwise, it is set to 0 (i.e., M-register is tested).
- If bit n in the first mask field is 0 and the same bit in the second mask field is 0, the corresponding bit in the M-register is neither modified nor tested.

> NOTE: The assembly language instructions LEV, SAVE, and STM store the contents of the M-register in a form suitable for reloading by MTM.

No indicators are affected. The address syllable can specify a memory location, an immediate operand, or a R-register. The register number in the M-number field must be 1; otherwise traps to trap vector #5.

MUL

Instruction:
Multiply R-register

Type:
Double Operand

Format:

```
 0  1      3  4        8  9              15
+--+------+--+--+--+--+--+----------------+
|1 |  Rn  |1 |0 |1 |1 |0 | address syllable|
+--+------+--+--+--+--+--+----------------+
|              optional                   |
+- - - - - - - - - - - - - - - - - - - - -+
```

Description:
Multiplies the word in the designated R-register by the word in the effective address. The product is a 16-bit value with the high order bits truncated unless R7 is specified, in which case a double precision 32-bit signed product is developed in R6 and R7. Single precision multiplication will set or reset the overflow (OV) indicator depending on the size of the product; double precision multipli-

cation cannot cause overflow and thus OV will be reset.

The address syllable can specify a memory location, an immediate operand, or another R-register.

The contents of the I-register are affected as follows:

- If the product is more than 2^{15} -1 (32767) or less than -2^{15} (-32768), the OV-bit is set to 1; otherwise, it is set to 0.
- If, during the multiplication, a carry occurs, the C-bit is set to 1; otherwise, it is set to 0.

NEG

Instruction:
Negate

Type:
Single Operand

Format:

0	1		3	4			8	9			15
1	0	0	0	0	0	1	0	0	address syllable		
				optional							
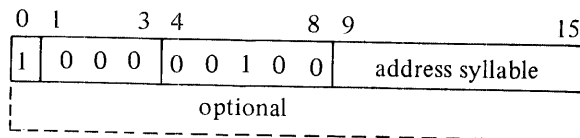
Description:
Two's complements the contents of the location specified in the address syllable.

The contents of the I-register are affected as follows:

- If a carry occurs during the operation, the C-bit is set to 1; otherwise, it is set to 0.
- If the value complemented was -32768, the OV-bit is set to 1; otherwise, it is set to 0. However, this cannot cause an overflow trap.

The address syllable can specify a memory location, an immediate operand, or one of the R-registers.

NOP

Instruction:
No operation

Type:
Branch on Indicator

Format:

0	1		3	4				8	9		15
0	0	0	0	1	1	1	1	0	address syllable		
					optional						
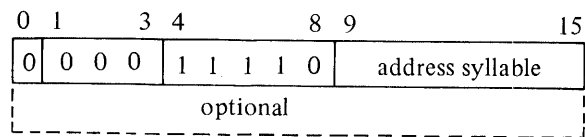
Description:
Performs no operation. In effect, it is the opposite of an unconditional branch (B) instruction.

OR

Instruction:
Inclusive OR with R-register

Type:
Double Operand

Format:

0	1		3	4				8	9		15
1		Rn		0	1	0	0	0	address syllable		
					optional						
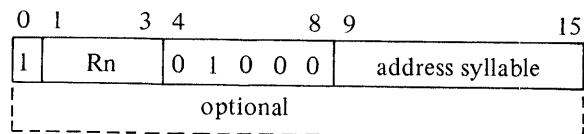
Description:
Logically OR's the word at the effective address to the word contained in the designated R-register. No indicators are affected. The address syllable can specify a memory address, an immediate operand, or another R-register.

The following chart illustrates the result of inclusively ORing bits:

First operand bit	0	0	1	1
Second operand bit	1	0	1	0
Result	1	0	1	1

Examples:

R-register (before)	Effective Address	R-register (after)
$(0000)_{16}$	$(0007)_{16}$	$(0007)_{16}$
$(FFF0)_{16}$	$(0007)_{16}$	$(FFF7)_{16}$
$(FFF3)_{16}$	$(0007)_{16}$	$(FFF7)_{16}$

ORH

Instruction:
Half-word (byte) inclusive OR with R-register

Type:
Double Operand

Format:

```
 0 1    3 4      8 9            15
┌─┬─────┬─────────┬───────────────┐
│1│ Rn  │0 1 0 0 1│address syllable│
├─┴─────┴─────────┴───────────────┤
│           optional              │
└─────────────────────────────────┘
```
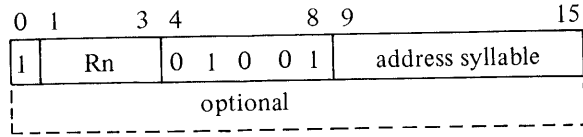
Description:

Logically OR's the byte at the effective address (with its sign extended) to the word contained in the designated R-register. No indicators are affected. The address syllable can specify a memory address, an immediate operand, or another R-register, with the byte being positioned as follows:
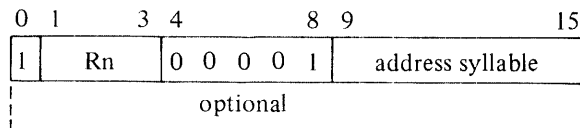
— memory location, not indexed   — left byte
— memory location, indexed —
    index value even   — left byte
    index value odd   — right byte
— immediate operand   — left byte
— R-register   — right byte

The following chart illustrates the result of inclusively ORing bits:

First operand bit	0	0	1	1
Second operand bit	1	0	1	0
Result	1	0	1	1

Examples:

R-register (before)	Effective Address	R-register (after)
$(0000)_{16}$	$(07)_{16}$	$(0007)_{16}$
$(FFF0)_{16}$	$(07)_{16}$	$(FFF7)_{16}$
$(FFF3)_{16}$	$(07)_{16}$	$(FFF7)_{16}$
$(0007)_{16}$	$(87)_{16}$	$(FF87)_{16}$

RSTR

Instruction:
Restore context

Type:
Single Operand

Format:

```
 0 1    3 4      8 9            15
┌─┬───┬─────────┬───────────────┐
│1│0 0 0│1 1 1 1 1│address syllable│
├─┴───┴─────────┴───────────────┤
│           optional            │
├───────────────────────────────┤
│             mask              │
└───────────────────────────────┘
```
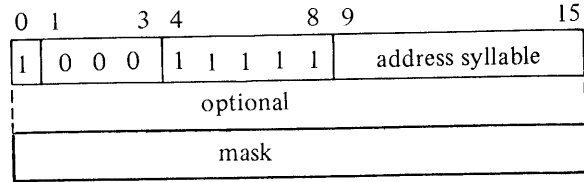
Description:

Restores the registers specified in the second operand mask starting from the location specified in the address syllable.

The address syllable must specify a memory location.

The second operand is a mask that specifies which registers are to be restored. If the mask is all zeros, the contents of R1 are used as the mask.

Depending on which bits in the specified mask are set to 1, the registers that can be restored are as follows:

Bit: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

M	R1	R2	R3	R4	R5	R6	R7	I	B1	B2	B3	B4	B5	B6	B7
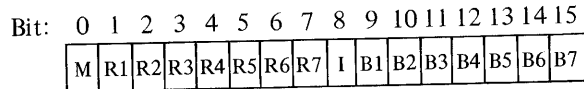
This mask should be the same as the one used to save the registers (see the SAVE instruction).

RTCF

Instruction:
Real-time clock off

Type:
Generic

Format:

```
 0              7 8            15
┌───────────────┬───────────────┐
│0 0 0 0 0 0 0 0│0 0 0 0 1 0 1│
└───────────────┴───────────────┘
```
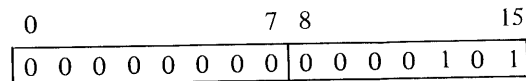
Description:

Disables real-time clock.

The P-bit in the S-register must be set to 1 (i.e., the central processor must be in the privileged state) for this instruction to be executed. If not, the unprivileged use of a privileged operation is signified by a trap to trap vector #13.

RTCN

Instruction:
Real-time clock on

Type:
Generic

Format:

```
0                  7 8              15
| 0 0 0 0 0 0 0 0 | 0 0 0 0 1 0 0 |
```
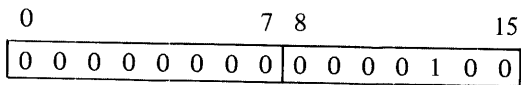
Description:

Starts the real-time clock.

The P-bit in the S-register must be set to 1 (i.e., the central processor must be in the privileged state) for this instruction to be executed. If not, the unprivileged use of a privileged operation is signified by a trap to trap vector #13.

RTT

Instruction:

Return from trap

Type:

Generic

Format:

```
0                  7 8              15
| 0 0 0 0 0 0 0 0 | 0 0 0 0 0 1 1 |
```
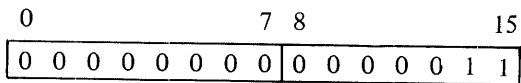
Description:

Restores the registers that were saved in the trap save area when the trap was entered; restores the central processor to the privileged state only if both the interrupted state and the interrupt handler executing the RTT are privileged; returns the trap save area block to the trap save area memory pool; returns control to the next instruction to be executed (determined by the event that caused the trap).

SAL

Instruction:

Single-shift arithmetic-left

Type:

Shift Short
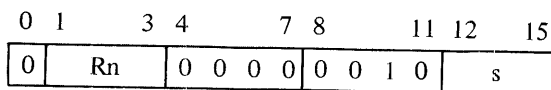
Format:

```
0 1       3 4      7 8      11 12   15
| 0 | Rn | 0 0 0 0 | 0 0 1 0 |   s   |
```
s is number of positions shifted (0-15)

Description:

Shifts the contents of the R-register identified in the Rn field left the number of bit positions specified in the s field. The bit positions vacated by the shift are filled with binary 0's.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

The contents of the I-register are affected as follows:

● If the contents of bit 0 in the R-register change, the OV-bit is set to 1; otherwise, it is set to 0.
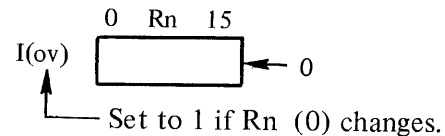
Pictorial Representation:

Set to 1 if Rn (0) changes.

SAR

Instruction:

Single-shift arithmetic-right

Type:

Shift Short
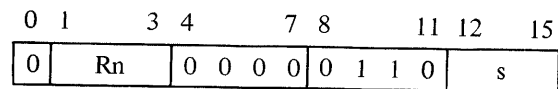
Format:

```
0 1       3 4      7 8      11 12   15
| 0 | Rn | 0 0 0 0 | 0 1 1 0 |   s   |
```
s is number of positions shifted (0-15)

Description:

Shifts the contents of the R-register identified in the Rn field right the number of bit positions specified in the s-field. The bit positions vacated by the shift are filled with the sign value originally contained in bit 0.

The contents of the I-register are affected as follows:

● C-bit contains the last binary digit shifted out of the R-register.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

Pictorial Representation:

Saves last bit shifted out of Rn(15)
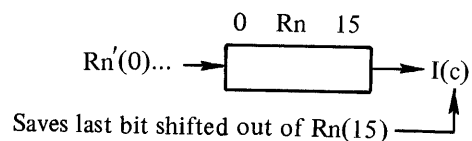
SAVE

Instruction:
Save context

Type:
Single Operand

Format:

```
 0  1    3 4       8 9            15
┌─┬──────┬─────────┬──────────────────┐
│1│0 0 0 │1 1 1 1 0│ address syllable │
├─┴──────┴─────────┴──────────────────┤
┊            optional                 ┊
├─────────────────────────────────────┤
│               mask                  │
└─────────────────────────────────────┘
```
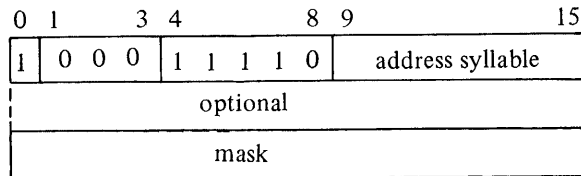
Description:

Saves the registers specified in the second operand starting at the location specified in the address syllable.

The address syllable must specify a memory address.

The second operand is a mask that specifies which registers are to be saved. Each bit in the mask represents a particular register which can be saved, as shown below:

```
Bit:  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15
     ┌─┬──┬──┬──┬──┬──┬──┬──┬─┬──┬──┬──┬──┬──┬──┬──┐
     │M│R1│R2│R3│R4│R5│R6│R7│I│B1│B2│B3│B4│B5│B6│B7│
     └─┴──┴──┴──┴──┴──┴──┴──┴─┴──┴──┴──┴──┴──┴──┴──┘
```
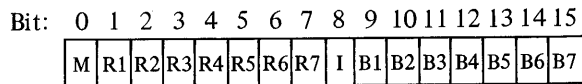
If a mask bit is set to 1, the corresponding register is saved. If a mask bit is 0, the corresponding register is not saved. If the mask is all zeros, the contents of R1 are used as the mask.

The registers are saved in reverse order. For example, if the second operand specified X'CA01' (which, when translated into binary is 1100 1010 0000 0001), indicating that registers M, R1, R4, R6, and B7 are to be saved, the context save area will contain the registers starting with B7 and ending with M.

SCL

Instruction:
Single-shift closed-left
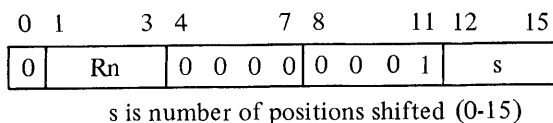
Type:
Shift Short

Format:

```
 0  1    3 4      7 8      11 12    15
┌─┬──────┬────────┬────────┬──────────┐
│0│  Rn  │0 0 0 0 │0 0 0 1 │    s     │
└─┴──────┴────────┴────────┴──────────┘
```

s is number of positions shifted (0-15)

Description:

Shifts the contents of the R-register identified in the Rn field left the number of bit positions specified in the s field. The bits shifted out of the register are placed in the bit positions vacated by shifted bits as they are shifting.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

Pictorial Representation:

SCR

Instruction:
Single-shift closed-right
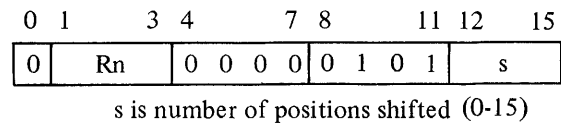
Type:
Shift Short

Format:

```
 0  1    3 4      7 8      11 12    15
┌─┬──────┬────────┬────────┬──────────┐
│0│  Rn  │0 0 0 0 │0 1 0 1 │    s     │
└─┴──────┴────────┴────────┴──────────┘
```

s is number of positions shifted (0-15)

Description:

Shifts the contents of the R-register identified in the Rn field right the number of bit positions specified in the s field. The bits shifted out of the register are placed in the bit positions vacated by shifted bits as they are shifting.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

Pictoral Representation:
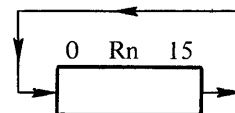
SOL

Instruction:
Single-shift open-left

Type:
Shift Short
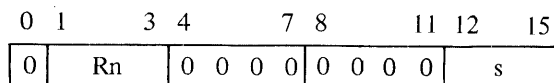
Format:

```
 0  1      3 4      7 8     11 12    15
┌─┬───────┬─────────┬─────────┬───────┐
│0│  Rn   │0 0 0 0 │0 0 0 0 │   s   │
└─┴───────┴─────────┴─────────┴───────┘
```

s is number of positions shifted (0-15)

Description:

Shifts the contents of the R-register identified in the Rn field left the number of bit positions specified in the s field. The bit positions vacated by the shift are filled with binary 0's.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

The contents of the I-register are affected as follows:

- C-bit contains the last binary digit shifted out of the R-register.

Pictorial Representation:

Saves last bit shifted out of Rn(0)
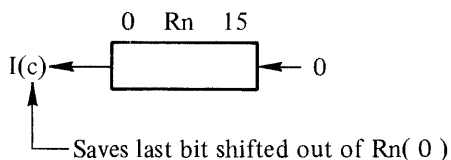
SDI

Instruction:
Store double word integer

Type:
Single Operand

Format:

```
 0  1    3 4        8 9              15
┌─┬──────┬───────────┬──────────────────┐
│1│0 0 0 │1 1 0 1 0 │ address syllable │
└─┴──────┴───────────┴──────────────────┘
┌────────────── optional ──────────────┐
└───────────────────────────────────────┘
```
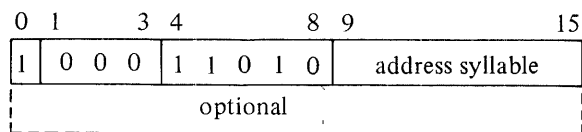
Description:

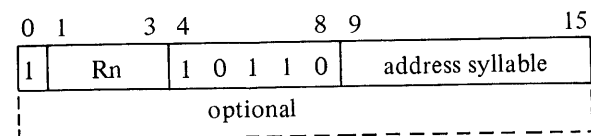Stores the contents of R6 and R7 into the effective address and the following word. No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another R-register as follows:

- Memory location: The left-hand word of a double-word pair will be addressed. Auto-increment and auto-decrement modes of addressing will add (subtract) two from the base register. A value in the index register

will count double words; it is shifted one place to the left before being applied. Auto-indexing will cause one to be added (subtracted) from the index register.

- Immediate operand: This will be a double-word operand and thus the instruction will be three words in length.
- Register operand: This form of addressing must address the right-hand register containing a double-word pair, i.e., either R3, which causes the contents of R6 and R7 to be stored in R2 and R3, or R5, which selects R4 and R5.

SOR

Instruction:
Single-shift open-right

Type:
Shift Short
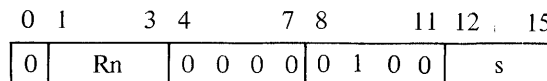
Format:

```
 0  1      3 4      7 8     11 12    15
┌─┬───────┬─────────┬─────────┬───────┐
│0│  Rn   │0 0 0 0 │0 1 0 0 │   s   │
└─┴───────┴─────────┴─────────┴───────┘
```

s is number of positions shifted (0-15)

Description:

Shifts the contents of the R-register identified in the Rn field right the number of bit positions specified in the s field. The bit positions vacated by the shift are filled with binary 0's.

The contents of the I-register are affected as follows:

- C-bit contains the last binary digit shifted out of the R-register.

If the s field contains 0's, the shift distance is obtained from bits 12 through 15 of general register R1.

Pictorial Representation:

Saves last bit shifted out of Rn(15)
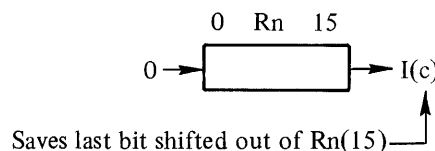
SRM

Instruction:
Store register masked

Type:
Double Operand

Format:

```
0  1      3  4        8  9                    15
┌──┬────────┬──────────┬──────────────────────┐
│1 │  Rn    │1  0  1  0  1│  address syllable   │
├──┴────────┴──────────┴──────────────────────┤
│                optional                      │
├──────────────────────────────────────────────┤
│                  mask                        │
└──────────────────────────────────────────────┘
```
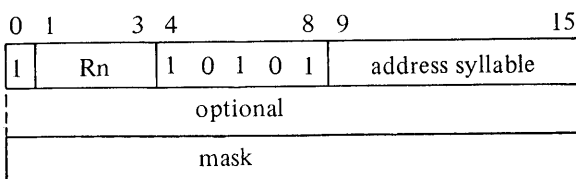
Description:
The contents of the designated register are stored in the effective address under control of a 16-bit mask. Every bit (zero or one) in the register with a corresponding mask bit of one is stored; those corresponding to zero bits in the mask are not transferred and the original bits in the effective address remain unchanged.

The mask is contained in the word following the instruction. If it is all zeros, the contents of R1 are used as a mask. If R1 also contains all zeros, the instruction does no operation.

No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another R-register.

Example: Contents of:

Register	Mask	Effective Address (before)	Effective Address (after)
$(ABCD)_{16}$	$(00FF)_{16}$	$(1234)_{16}$	$(12CD)_{16}$
$(ABCD)_{16}$	$(1111)_{16}$	$(1234)_{16}$	$(0325)_{16}$

STB

Instruction:
Store B-register

Type:
Double Operand

Format:

```
0  1      3  4        8  9                    15
┌──┬────────┬──────────┬──────────────────────┐
│1 │  Bn    │1  1  1  1  1│  address syllable   │
├──┴────────┴──────────┴──────────────────────┤
│                optional                      │
└──────────────────────────────────────────────┘
```
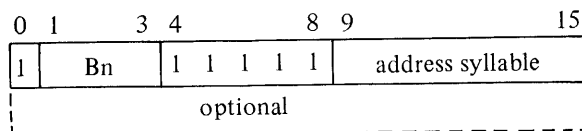
Description:
Stores the word contained in the designated B-register into the location specified by the effective address. No indicators are affected. The

address syllable can specify a memory location, an immediate operand, or another B-register.

STH

Instruction:
Store R-register halfword (byte)

Type:
Double Operand

Format:

```
0  1      3  4        8  9                    15
┌──┬────────┬──────────┬──────────────────────┐
│1 │  Rn    │0  1  1  1  1│  address syllable   │
├──┴────────┴──────────┴──────────────────────┤
│                optional                      │
└──────────────────────────────────────────────┘
```
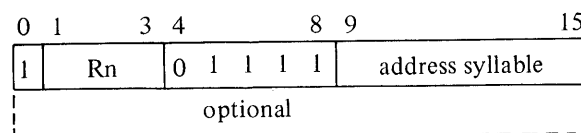
Description:
Stores the right-hand byte of the designated R-register into the half-word specified by the effective address. The other half is not changed. No indicators are affected.

The effective address can specify a memory location, an immediate operand, or another R-register, with the byte being positioned as follows:

— memory location, not indexed	— left byte
— memory location, indexed index value even	— left byte
index value odd	— right byte
— immediate operand	— left byte
— R-register	— right byte

Example: Assume that:

— register B1	contains 1000
— register R1	contains 0
— register R2	contains 1
— register R5	contains (ABCD)
— location 1000	contains $(1234)_{16}$

then if STH $R5, $B1.$R1 is executed:

— location 1000 will contain $(CD34)_{16}$

but if STH $R5,$B1.$R2 is executed:

— location 1000 will contain $(12CD)_{16}$

STM

Instruction:
Store M-register

Type:
Double Operand

Format:

0	1	3	4				8	9	15
1	M1		0	1	1	1	0	address syllable	

optional
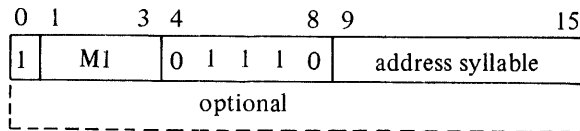
Description:
Stores the 8-bit M-register identified in the first operand in the right half-word of the location specified in the address syllable; the left half-word of the location is filled with 1's.

The address syllable can specify a memory location, an immediate operand, or one of the R-registers.

STR

Instruction:
Store R-register

Type:
Double Operand
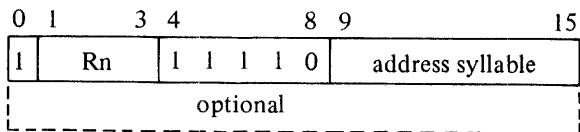
Format:

0	1	3	4				8	9	15
1	Rn		1	1	1	1	0	address syllable	

optional

Description:
Stores the word contained in the designated R-register into the location specified by the effective address. No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another R-register.

STS

Instruction:
Store S-register

Type:
Single Operand

Format:

0	1		3	4				8	9	15
1	0	0	0	1	1	0	0	0	address syllable	
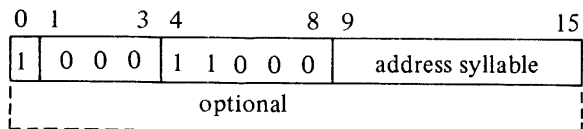
optional

Description:
The contents of the status register are stored in the location specified by the effective address.

No indicators are affected. The address syllable can specify a memory location, an immediate operand, or an R-register.

SUB

Instruction:
Subtract from R-register

Type:
Double Operand

Format:

0	1	3	4				8	9	15
1	Rn		0	0	1	0	0	address syllable	

optional
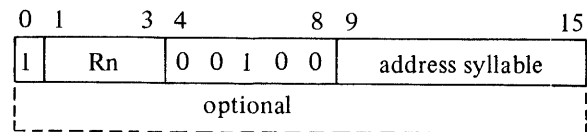
Description:
Subtracts the word at the effective address from the word contained in the designated R-register. The carry (C) and overflow (OV) indicators will be set if carry and/or overflow occurs respectively; otherwise they will be reset to zero. The address syllable can specify a memory location, an immediate operand, or another R-register.

Some examples of subtraction:

R-register (before)	Effective Address (before & after)	R-register (after)	C (After)	OV (After)
−32767	+1	−32768	0	0
−32768	+1	+32767	1	1
−1	−1	0	1	0

SWB

Instruction:
Swap B-register

Type:
Double Operand
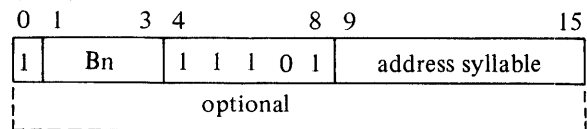
Format:

0	1	3	4				8	9	15
1	Bn		1	1	1	0	1	address syllable	

optional

Description:

Swaps the word contained in the designated B-register with the word at the effective address. No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another B-register.

SWR

Instruction:

Swap R-register

Type:

Double Operand
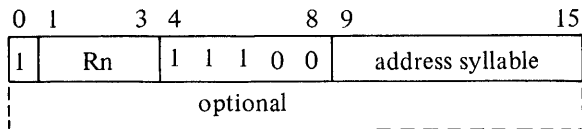
Format:

```
0  1      3 4      8 9            15
| 1 |  Rn  | 1 1 1 0 0 | address syllable |
|--------- optional ---------------------|
```

Description:

Swaps the word contained in the designated R-register with the word at the effective address. No indicators are affected. The address syllable can specify a memory location, an immediate operand, or another R-register.

WDTF

Instruction:

Watchdog timer off (optional)

Type:

Generic

Format:

```
0              7 8            15
| 0 0 0 0 0 0 0 0 | 0 0 0 0 1 1 1 |
```
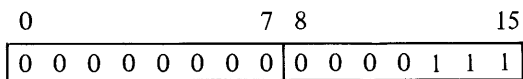
Description:

Disables the watchdog timer.

The P-bit in the S-register must be set to 1 (i.e., the central processor must be in the privileged state) for this instruction to be executed. If note, the unprivileged use of a privileged operation is signified by a trap to trap vector #13.

WDTN

Instruction:

Watchdog timer on (optional)

Type:

Generic

Format:

```
0              7 8            15
| 0 0 0 0 0 0 0 0 | 0 0 0 0 1 1 0 |
```
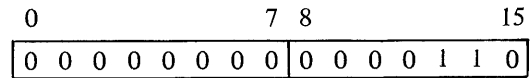
Description:

Enables watchdog timer.

The P-bit in the S-register must be set to 1 (i.e., the central processor must be in the privileged state) for this instruction to be executed. If not, the unprivileged use of a privileged operation is signified by a trap to trap vector #13.

XOH

Instruction:

Half-word (byte) exclusive OR with R-register

Type:

Double Operand

Format:

```
0  1      3 4      8 9            15
| 1 |  Rn  | 0 1 1 0 1 | address syllable |
|--------- optional ---------------------|
```
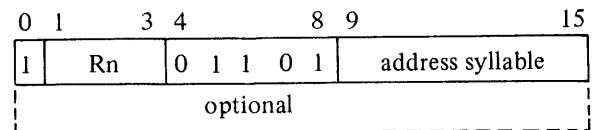
Description:

Logically "exclusive OR's" the byte at the effective address (with sign extended) to the word contained in the designated R-register. No indicators are affected. The address syllable can specify a memory address, an immediate operand, or another R-register, with the byte being positioned as follows:

— memory location, not indexed	— left byte
— memory location, indexed	
index value even	— left byte
index value odd	— right byte
— immediate operand	— left byte
— R-register	— right byte

The following chart illustrates the result of exclusively ORing bits:

First operand bit	0	0	1	1
Second operand bit	1	0	1	0
Result	1	0	0	1

XOH

Examples:

R-register (before)	Effective Address	R-register (after)
$(0000)_{16}$	$(07)_{16}$	$(0007)_{16}$
$(0007)_{16}$	$(07)_{16}$	$(0000)_{16}$
$(FFFF)_{16}$	$(88)_{16}$	$(0077)_{16}$

XOR

Instruction:
Exclusive OR with R-register

Type:
Double Operand

Format:

0	1	3	4				8	9		15
1	Rn		0	1	1	0	0	address syllable		
	optional									
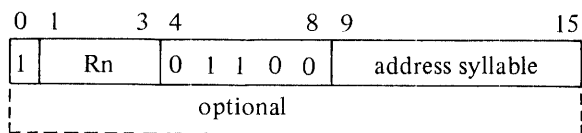
Description:
Logically "exclusive OR's" the word at the effective address to the word contained in the designated R-register. No indicators are affected. The address syllable can specify a memory address, an immediate operand, or another R-register.

The following chart illustrates the result of exclusively ORing bits:

First operand bit	0	0	1	1
Second operand bit	1	0	1	0
Result	1	0	0	1

Examples:

R-register (before)	Effective Address	R-register (after)
$(0000)_{16}$	$(0007)_{16}$	$(0007)_{16}$
$(0007)_{16}$	$(0007)_{16}$	$(0000)_{16}$
$(FFFF)_{16}$	$(8888)_{16}$	$(7777)_{16}$

SECTION 5

CONTROL PANEL

The full control panel is used for powering up and initializing the system, starting and stopping the central processor, entering and displaying registers and memory, single stepping a program, bootloading a program, clearing the system, and indicating CP status. The panel layout is shown in Figure 5-1. Its six major functional elements are:

Power switch
Control panel keylock
Control keys
Status indicator lights
Register display
Register keys (hex pad)

POWER SWITCH AND CONTROL PANEL KEYLOCK

Power switch	Up for power on
	Down for power off
Keylock	Right for panel locked
	Left for panel unlocked
	When panel is locked, all panel switches and keys, except power switch, are inoperable, and the register display is disabled.

CONTROL KEYS

These are 11 touch keys for controlling processor states and modes (see Table 5-1).

TABLE 5-1. CONTROL KEYS

Key	Function	Color[a]	Description
L	Load	green	Depress to place the processor in load mode and to bootload a program into memory.
C	Change	green	Depress to place the processor in change mode. In this mode the processor is ready to accept operator modifications to the contents of the selected register.
1	Plus 1	white	Depress to place the processor in plus-1 mode. In this mode the processor is ready to read or write successive memory locations from the control panel, and each depression of the E key causes the memory address register to be incremented by one.
W	Write	white	Depress to place the processor in write mode. In this mode the processor writes the contents of the selected register into the location addressed by memory address register A0.

[a]Refers to legend on key.

Figure 5-1. Full Control Panel Layout

TABLE 5-1 (cont). CONTROL KEYS

Key	Function	Color	Description
R	Read	white	Depress to place the processor in read mode. In this mode the processor reads the contents of the selected register from the location addressed by memory address register A0.
S	Stop	red	Depress to stop instruction execution and place the processor in stop state.
R	Ready	red	Depress to place the processor in ready mode. In this mode the processor is ready to execute.
CLR	Master CLeaR	black	Depress to clear the processor. This action resets the instruction register D0 and the program counter E0 to zero and clears any order pending in the processor. Master clear can be performed only in the stop state.
S	Select	green	Depress to place the processor in the select mode. The register to be operated on is selected by keying in the proper selection code from the hex pad.
0	Plus 0	white	Depress to reset the plus-1 mode. In this mode the memory address register cannot be modified during a memory read or write.

TABLE 5-1 (cont). CONTROL KEYS

Key	Function	Color	Description
E	Execute	black	Depress to put the processor in the run state. In this state the processor executes instructions, starting at the location specified by the program counter. Execution continues until the S key is depressed or up to the first halt instruction.

STATUS INDICATOR LIGHTS

Eleven lights in the portion of the panel labeled MONITOR indicate status and operating modes (see Table 5-2).

TABLE 5-2. STATUS INDICATOR LIGHTS

Indicator	Description
DC ON	Lights to indicate DC power is on.
CHECK	Lights to indicate a bus element has not successfully completed its logic tests (BLT) or a bus element is not plugged into the bus properly.
TRAFFIC	Lights to indicate the processor is executing instructions other than the halt instruction.
RUN	Lights to indicate the processor is in run state; i.e., it is executing a program. If the TRAFFIC light is off while the RUN light is on, the processor is in a halt.
LOAD	Lights when L key is depressed.
CHANGE	Lights when C key is depressed.
PLUS	Lights when plus-1 key is depressed. The light goes off when the reset-to-0 key is depressed.
WRITE	Lights when W key is depressed.
READ	Lights when white R key is depressed.
STOP/STEP	Lights when red S key is depressed.
READY	Lights when red R key is depressed. Depress the E key to run.

REGISTER DISPLAY

A six-digit hexadecimal (hex) display in the upper part of the panel marked REGISTER indicates the two-digit LOCATION and four-digit CONTENTS of any one of twenty-one registers. Figure 5-2 shows the codes for selecting registers. For descriptions of these registers, see Section 3.

REGISTER KEYS (HEX PAD)

The set of sixteen hexadecimal keys in the right part of the control panel marked REGISTERS is called the hex pad. These keys provide access to the twenty-one user-visible registers.

In the select mode, a hex pad key-in selects the register to be operated on, and the digits entered light up under LOCATION in the Register Display.

In the change mode, a hex pad key-in changes the contents of the selected register, and the digits entered light up under CONTENTS in the Register Display. Each keystroke shifts and loads one hexadecimal digit into the least significant hexadecimal position of the selected register and the display.

		0	15
D	0	INSTRUCTION REGISTER	
D	1	R1	
D	2	R2	
D	3	R3	
D	4	R4	
D	5	R5	
D	6	R6	
D	7	R7	
E	0	P-REGISTER	
B	1	B1	
B	2	B2	
B	3	B3	
B	4	B4	
B	5	B5	
B	6	B6	
B	7	B7	
B	0	MEMORY DATA REGISTER	
A	0	MEMORY ADDRESS REGISTER	
C	1	M1 REGISTER	I-REGISTER
E	7	S-REGISTER	

Figure 5-2. Register Selection Codes

SECTION 6

PERIPHERAL DEVICES

This section describes the functional characteristics, features, operational capabilities, and programming for the various peripheral devices listed in Table 6-1. All of the devices are supported by the Level 6 GCOS/BES I/O drivers

TABLE 6-1. LEVEL 6 PERIPHERAL DEVICES

Device	Description
Card Readers	
CRU9101/9103	300/500 cpm punched card readers
CRU9102/9104	300/500 cpm punched card and marked sense readers
Consoles	
TTU9101/9102	10 cps, 72 characters per line, ASR-/KSR-33
TWU9101	30 cps, 132 characters per line, 64-character ASCII set
DKU9101	960 character display (12 lines, 80 characters per line)
Disk Devices	
DIU9101/9102	Single/Dual diskettes, 401,016 bytes/disk (unformatted), 256, 256 bytes/disk (formatted)
CDU9101	Cartridge Disk Unit, low-density, 2.5 MB, removable disk only
CDU9102	Cartridge Disk Unit, low-density, 5.0 MB, fixed and removable disks
CDU9103	Cartridge Disk Unit, high-density, 5.0 MB, removable disk only
CDU9104	Cartridge Disk Unit, high-density 10.0 MB, fixed and removable disks
Printers	
PRU9101/9102	Serial Printers, 60 lpm, 64-/96-ASCII character set
PRU9103/9104	Line Printers, 240 lpm/300 lpm, 96-/64-ASCII character set
PRU9105/9106	Line Printers, 480 lpm/600 lpm, 96-/64-ASCII character set

and executive routines. Test and maintenance programs are also provided to assist in fault isolation and maintenance of the equipment.

PERIPHERAL DEVICE CONNECTION

Peripheral device connection to the Level 6 Megabus occurs via a single-board Multiple Device Controller (MDC9101) and an appropriate Device-Pac (see Figure 6-1). The MDC provides four levels of simultaneity (supporting up to four devices in any combination) with full DMA. The Device-Pac contains all the necessary hardware to interface the peripheral device. The MDC may connect any of those devices listed in Table 6-1 with the exception of the Cartridge Disk Units which require the MSC9101 Mass Storage Controller.
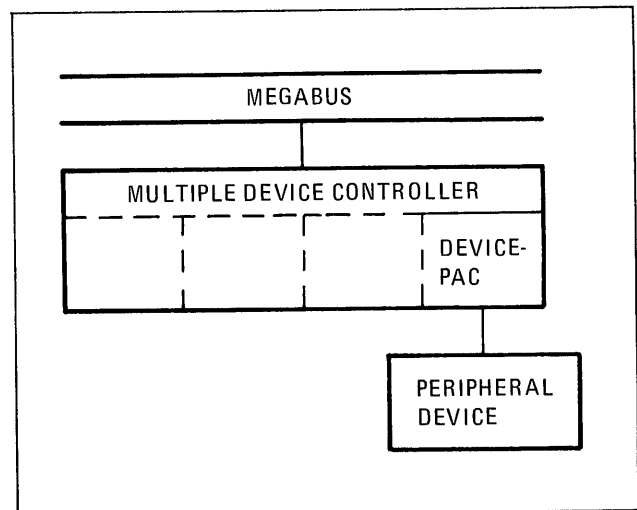
Figure 6-1. Peripheral Device Connection

MDC Internal Memory and Command Interpretation

Internal to the MDC is a 256 byte Read/Write (R/W) memory (64 bytes of this memory are dedicated to each channel of the MDC). The memory is used for all active storage in the MDC relative to a specific channel. Included are the DMA address, range, interrupt level, status and other internal MDC working storage. The CP has the ability to read or write any location in the R/W memory so long as the specific channel is not busy. In order to write a memory location, an I/O output command is used, whereas reading is done with an I/O input command. Addressing of the R/W Memory relates to the I/O command as follows:

```
0                    7 8          17 18      23
┌──────────────────┬───────────────┬──────────┐
│ ZERO EXCEPT FOR  │               │ FUNCTION │
│  FC = 09 WHICH   │ CHANNEL NUMBER│  CODE    │
│ LOADS ADDRESS    │               │          │
└──────────────────┴───────────────┴──────────┘
                     15 16 17 18  22 23
```

THESE 2 BITS IDENTIFY WHICH
MDC PORT IS BEING ADDRESSED

DIRECTION BIT   0 = READ (INPUT)
                 1 = WRITE (OUTPUT)

THESE 5 BITS
IDENTIFY THE
BYTE PAIR IN
MDC MEMORY

1 = WRITE MDC
    MEMORY
0 = READ MDC
    MEMORY

DATA BUS
```
0                 7 8                      15
┌──────────────────┬──────────────────────┐
│                  │                      │
└──────────────────┴──────────────────────┘
```

THESE 16 BITS WILL CONTAIN THE
BYTE PAIR IN MDC MEMORY
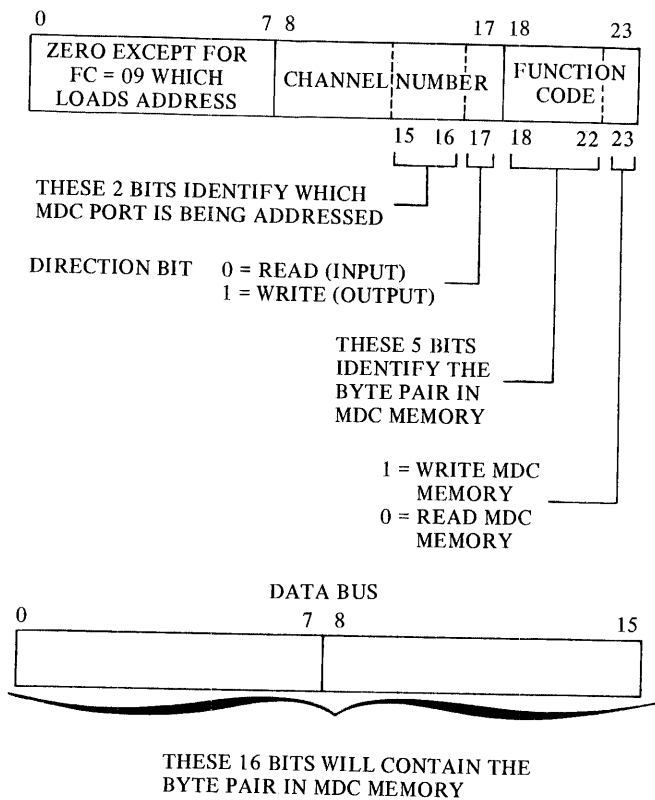
The format shown is for a Write cycle on the bus. For a Read cycle, the memory data will be returned from the MDC on a second bus transfer. It can be seen that all of the defined function codes for each peripheral device represents specific MDC memory locations.

The general response of the MDC/peripheral device to an I/O command is, therefore, only an updating of the designated memory location. Only two exceptions to this exist:

1. Function code 0D which is the range register and comes as part of an IOLD command is an implicit start I/O command. When an MDC peripheral device other than a diskette receives this function code, it assumes all the contents of its R/W memory are correct and executes the required operation. This function code will also cause the peripheral device to become busy. For diskette devices and devices on other controllers, the Output Task function code is used to initiate peripheral action. This function code (0D) will violate memory protection if used separately from the IOLD command.

2. Function code 01, which is Output Control, causes additional actions as described for each peripheral device.

The MDC treats Function Code 09 specially, in that a 24 bit address is to be loaded. In this case the 8 bit module number is written into the MDC R/W memory immediately following the location implied by 09 (i.e., 0B).

For the IOLD command (FC=09), the direction bit is a 1 for output or a 0 for input. For all other commands the direction bit is ignored.

Bus Responses and Busy Conditions

The command IOLD (FC=09) will cause a peripheral device to go busy and it will remain busy until after the interrupt has been acknowledged by the CP (see paragraph entitled "Interrupts"). If the interrupt level was set to Zero thus blocking the interrupts, the peripheral device will go non-busy immediately upon setting the status condition which would have caused an interrupt. During the time the peripheral device is busy, every I/O command will be NAK'd except for Output Control (Function Code 01).

Channel Number

The Channel Number for the MDC is separated into fields as follows:

```
                              Bit Definitions
                              Refer to Address
                              Bus
8                          14  15  16  17
┌──────────────────────────┬───────┬───┐
│  Switch Settable         │  MDC  │ D │
│     on MDC               │  Port │   │
└──────────────────────────┴───────┴───┘
```

Direction Bit
0 = Read (Input)
1 = Write (Output)
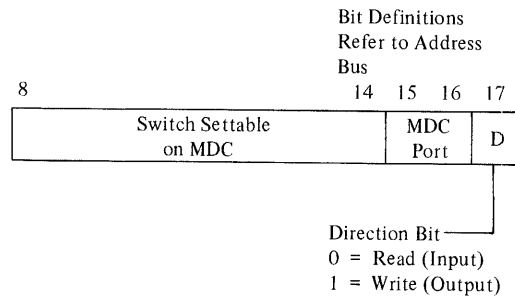
Bits 8 through 14 can have any value. The value selected will identify the entire MDC and, therefore, will affect other channel number selections for devices also connected to the MDC. Bits 15 and 16 identify which Device-Pac slot is occupied. Any or all of the four slots may be occupied. When different devices coexist on the MDC, the Device-Pac's physical position should be considered because the MDC services port #0 (bit 15, 16 = 00) at highest priority, and port #3 (bit 15, 16 = 11) at lowest priority. Bit 17 must be 0 for input and 1 for output.

Device Identification Number

In response to Function Code 26, the MDC (or MSC) will supply a 16 bit device identification number on the data bus. Table 6-2 lists the device ID numbers for the various peripheral devices.

TABLE 6-2. PERIPHERAL DEVICE ID NUMBERS

Peripheral Device	Device ID Number
Card Reader	2008 (CRU9101/9102/9103/ 9104)
Teleprinter	2018 (TTU9102)
	2019 (TTU9101)
CRT Keyboard Console	2020 (DKU9101)
Keyboard Typewriter Console	2018 (TWU9101)
Diskette	2010 (DIU9101/9102)
Cartridge Disk	2330 (CDU9101)
	2331 (CDU9102)
	2332 (CDU9103)
	2334 (CDU9104)
Serial Printer	2004 (PRU9101)
	2006 (PRU9102)
Line Printer	2000 (PRU9104/9106)
	2001 (same as above but with Option PRF9102)
	2002 (PRU9103/9105)
	2003 (same as above but with Option PRF9102)

Test Mode

When an Output Control Word command is received with the Test Mode bit on (while the MDC is in normal operating mode) the MDC will enter Test Mode and stop. Once the MDC is in Test Mode, subsequent commands will cause the contents of the Data Bus to be loaded into the MDC instruction register. The Data Bus contains the complement of a microinstruction. One clock pulse will then be issued to execute the microinstruction loaded. This enables a sequence of microinstructions to be executed in single step mode from a software test routine. Normal mode is resumed when a "reset test mode" microinstruction is executed or when Master Clear is activated on the Bus.

All function codes which are received over the Bus while the MDC is in Test Mode will cause the contents of the Data Bus to be loaded into the MDC instruction register as described above (function code field of the Address Bus is ignored). Note that response cycles will not be generated for Input commands (e.g., Input Status Word A).

Test Mode operates on an entire MDC and, therefore, precludes normal usage of other devices on the MDC at the same time.

CARD READERS

The Types CRU9101/9102/9103/9104 Card Readers are compact, self-contained, tabletop units providing economy and versatility of operation (Figure 6-2). The CRU9101/9102 and the CRU9103/9104 read 80-column Hollerith or binary punched cards at the rate of 300 and 500 cards per minute, respectively. In addition, the CRU9102 and 9104 have the capability of reading 40- or 80-column mark sense cards. In the mark sense mode, cards marked in either the same or alternate row position as punched card rows can be easily and quickly read. With Option CRF9101, the CRU9101/9102/9103/9104 Card Readers can have the capability of reading 51-column punched cards.

The card readers interface with the 6/30 Models by means of a single-board Multiple Device Controller (MDC9101), a Card Reader Device-Pac (CRM9101), and a 50-foot cable. A maximum of four card readers are connectable per MDC.

Features

- Convenient tabletop size
- Low cost
- Choice of 300 or 500 cpm reader
- Choice of versatile 80-column punched card and 40-/80-column mark sense readers or 80-column punched card readers
- Extremely simple operation – Power, Reset and Stop buttons on all four units; 40/80-column selector and mark sense/ punch selector on CRU9102/9104
- 500-card input hopper and output stacker capacity
- Status and error indication bits that can be read into the processor under program control for error detection and operator notification
- Empty hopper or full stacker signaled by Reset indicator (status transmitted to controller)
- Two program-selected punched card reading modes: ASCII with automatic Hollerith to eight-bit ASCII conversion; and Direct (Binary), with 12-bit binary format
- Test mode for easy maintenance

Operation

All data transfers are under DMA (Direct Memory Access) control, with an end-of-range interrupt after the program selected number of columns have been transferred.

While waiting for a ready indication, the central processor is free to perform other operations. Program interrupt is used to signal the central processor when further device servicing is required.
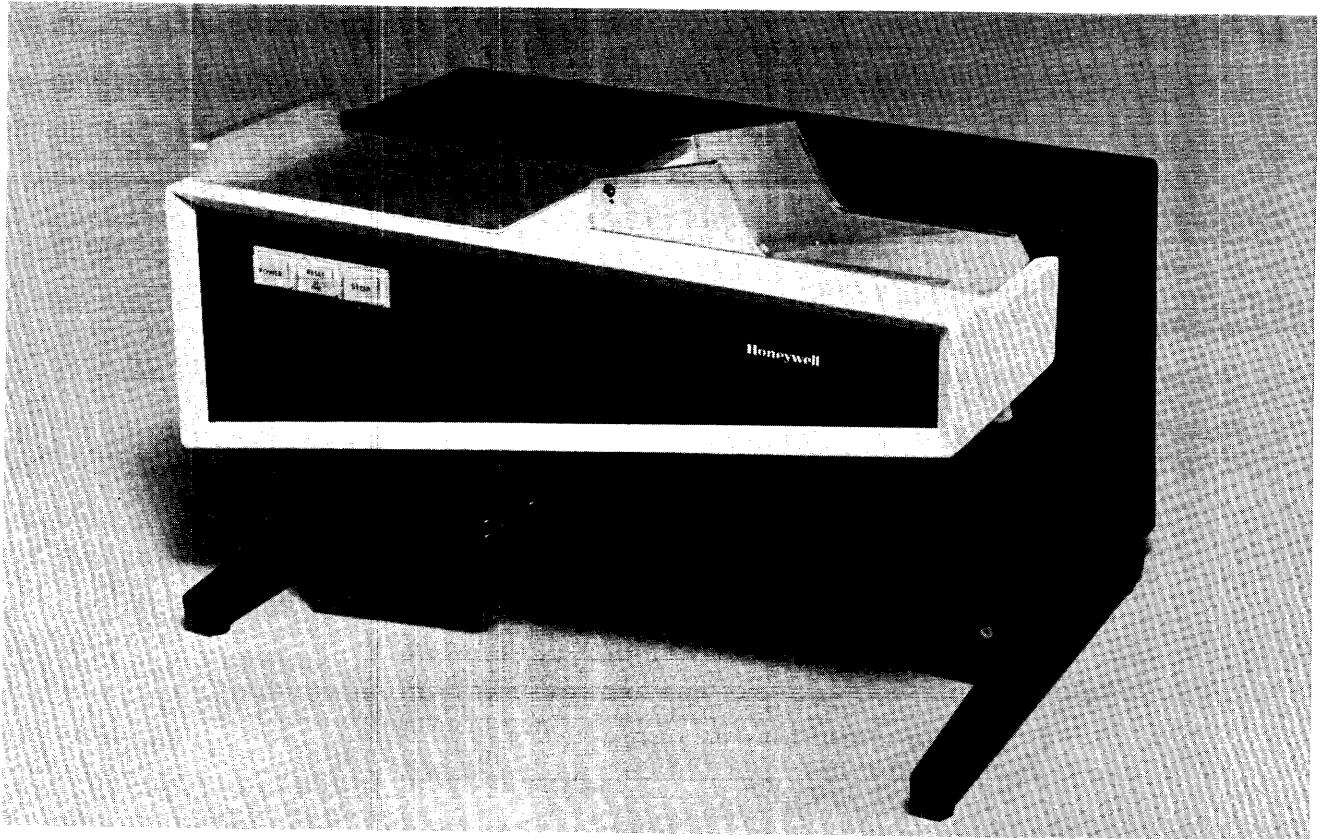
Figure 6-2. CRU9101/9102/9103/9104 Card Readers

Data Format

Cards may be read in either of two formats:

- Binary (Direct Transcription)
- ASCII

Binary Mode

In this mode, the 12 bits designated by each card column are placed on the data bus right justified, as shown in Figure 6-3, one memory word will be required for each card column read. All 2^{12} hole patterns will be valid in Binary Mode. The four remaining bits will be zero-filled.

ASCII Mode

In this mode, the 12 bits designated by each card column are converted to a single 8 bit byte and transferred to the bus, two bytes per word; see Figure 6-4. The conversion is a Hollerith to ASCII conversion and is performed by the Device-Pac. The code table of Table 6-3 completely describes the correspondence between the two codes. The bit designations in Table 6-3 are the ASCII standards and relate to the bits on the data bus as shown in Table 6-4. Punches or marks which do not exist in Table 6-3 will cause an ASCII error status report as described for bit 8 in Table 6-6.
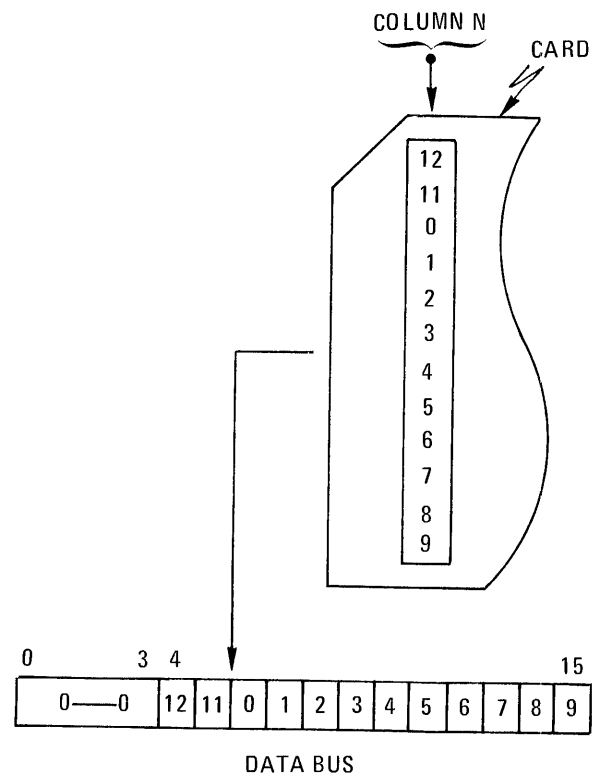
Figure 6-3. Binary Mode Format
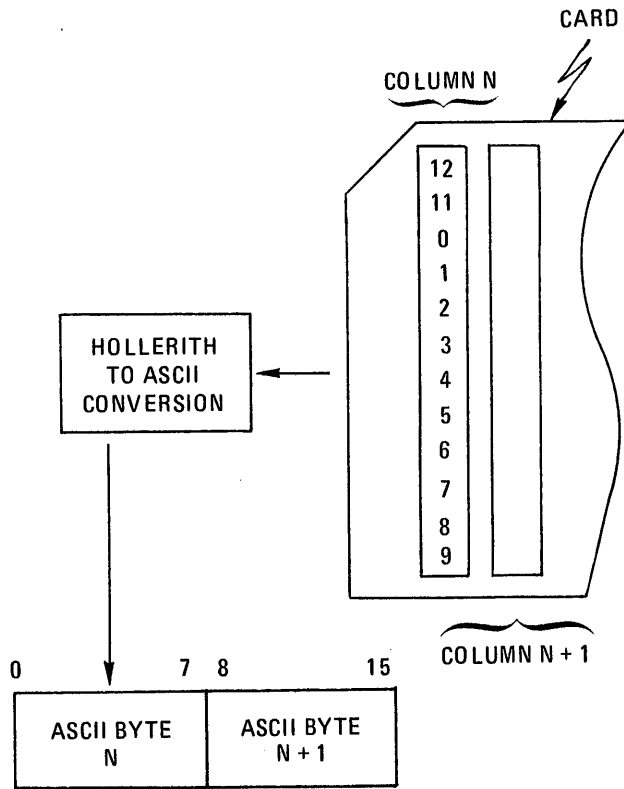
Figure 6-4. ASCII Mode Format

TABLE 6-3. HOLLERITH-ASCII CODE TABLE

b4b3b2b1 \ Row	0 b8b7b6b5 =0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	10 1010	11 1011	12 1100	13 1101	14 1110	15 1111	Col \ Row
0000 / 0	NUL 12-0-9-8-1	DLE 12-11-9-8-1	SP No Pch	0 0	@ 8-4	P 11-7	\ 8-1	p 12-11-7	11-0-9 8-1	12-11-0-9-8-1	12-0-9-1	12-11-9-8	12-11-0-9-6	12-11-8-7	12-11-0-8	12-11-9-8-4	0
0001 / 1	SOH 12-9-1	DC1 11-9-1	! ① 12-8-7	1 1	A 12-1	Q 11-8	a 12-0-1	q 12-11-8	0-9-1	9-1	12-0-9-2	11-8-1	12-11-0-9-7	11-0-8-1	12-11-0-9	12-11-9-8-5	1
0010 / 2	STX 12-9-2	DC2 11-9-2	" 8-7	2 2	B 12-2	R 11-9	b 12-0-2	r 12-11-9	0-9-2	11-9-8-2	12-0-9-3	11-0-9-2	12-11-0-9-8	11-0-8-2	12-11-0-8-2	12-11-9-8-6	2
0011 / 3	ETX 12-9-3	DC3 11-9-3	# 8-3	3 3	C 12-3	S 0-2	c 12-0-3	s 11-0-2	0-9-3	9-3	12-0-9-4	11-0-9-3	12-0-8-1	11-0-8-3	12-11-0-8-3	12-11-9-8-7	3
0100 / 4	EOT 9-7	DC4 9-8-4	$ 11-8-3	4 4	D 12-4	T 0-3	d 12-0-4	t 11-0-3	0-9-4	9-4	12-0-9-5	11-0-9-4	12-0-8-2	11-0-8-4	12-11-0-8-4	11-0-9-8-2	4
0101 / 5	ENQ 0-9-8-5	NAK 9-8-5	% 0-8-4	5 5	E 12-5	U 0-4	e 12-0-5	u 11-0-4	11-9-5	9-5	12-0-9-6	11-0-9-5	12-0-8-3	11-0-8-5	12-11-0-8-5	11-0-9-8-3	5
0110 / 6	ACK 0-9-8-6	SYN 9-2	& 12	6 6	F 12-6	V 0-5	f 12-0-6	v 11-0-5	12-9-6	9-6	12-0-9-7	11-0-9-6	12-0-8-4	11-0-8-6	12-11-0-8-6	11-0-9-8-4	6
0111 / 7	BEL 0-9-8-7	ETB 0-9-6	' 8-5	7 7	G 12-7	W 0-6	g 12-0-7	w 11-0-6	11-9-7	12-9-8	12-0-9-8	11-0-9-7	12-0-8-5	11-0-8-7	12-11-0-8-7	11-0-9-8-5	7
1000 / 8	BS 11-9-6	CAN 11-9-8	(12-8-5	8 8	H 12-8	X 0-7	h 12-0-8	x 11-0-7	0-9-8	9-8	12-8-1	11-0-9-8	12-0-8-6	12-11-0-8-1	12-0-9-8-2	11-0-9-8-6	8
1001 / 9	HT 12-9-5	EM 11-9-8-1	) 11-8-5	9 9	I 12-9	Y 0-8	i 12-0-9	y 11-0-8	0-9-8-1	9-8-1	12-11-9-1	0-8-1	12-0-8-7	12-11-0-1	12-0-9-8-3	11-0-9-8-7	9
1010 / 10	IF 0-9-5	SUB 9-8-7	* 11-8-4	: 8-2	J 11-1	Z 0-9	j 12-11-1	z 11-0-9	0-9-8-2	9-8-2	12-11-9-2	12-11-0	12-11-8-1	12-11-0-2	12-0-9-8-4	12-11-0-9-8-2	10
1011 / 11	VT 12-9-8-3	ESC 0-9-7	+ 12-8-6	; 11-8-6	K 11-2	[12-8-2	k 12-11-2	{ 12-0	0-9-8-3	9-8-3	12-11-9-3	12-11-0-9-1	12-11-8-2	12-11-0-3	12-0-9-8-5	12-11-0-9-8-3	11
1100 / 12	FF 12-9-8-4	FS 11-9-8-4	, 0-8-3	< 12-8-4	L 11-3	\ 0-8-2	l 12-11-3	| 12-11	0-9-8-4	12-9-4	12-11-9-4	12-11-0-9-2	12-11-8-3	12-11-0-4	12-0-9-8-6	12-11-0-9-8-4	12
1101 / 13	CR 12-9-8-5	GS 11-9-8-5	- 11	= 8-6	M 11-4	] 11-8-2	m 12-11-4	} 11-0	12-9-8-1	11-9-4	12-11-9-5	12-11-0-9-3	12-11-8-4	12-11-0-5	12-0-9-8-7	12-11-0-9-8-5	13
1110 / 14	SO 12-9-8-6	RS 11-9-8-6	. 12-8-3	> 0-8-6	N 11-5	∧ ② 11-8-7	n 12-11-5	~ 11-0-1	12-9-8-2	9-8-6	12-11-9-6	12-11-0-9-4	12-11-8-5	12-11-0-6	12-11-9-8-2	12-11-0-9-8-6	14
1111 / 15	SI 12-9-8-7	US 11-9-8-7	/ 0-1	? 0-8-7	O 11-6	_ 0-8-5	o 12-11-6	DEL 12-9-7	11-9-8-3	11-0-9-1	12-11-9-7	12-11-0-9-5	12-11-8-6	12-11-0-7	12-11-9-8-3	EO 12-11-0-9-8-7	15

① may be "|"
② may be "¬"
③ The top line in each entry to the table represents an assigned character (columns 0 to 7). The bottom line in each entry is the corresponding card hole-pattern.
④ All bit designations are in ASCII.

TABLE 6-4. ASCII BIT RELATION TO BITS ON DATA BUS

| ASCII Bit | Bus | |
	Left Byte	Right Byte
8	0	8
7	1	9
6	2	10
5	3	11
4	4	12
3	5	13
2	6	14
1	7	15

Instructions

Table 6-5 lists the I/O commands to which the MDC/card reader Device-Pac/card readers respond. A detailed description of each command follows this table.

TABLE 6-5. CARD READER COMMANDS

Type	Function Code	Command
Output	03	Output Interrupt Control
	01	Output Control
	09	Output Address and Range
	11	Output Configuration
Input	02	Input Interrupt Control
	08	Input Memory Byte Address
	0A	Input Memory Module Address
	0C	Input Range
	10	Input Configuration
	18	Input Status
	26	Input Device ID

Output Commands
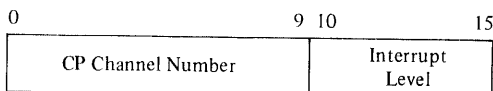
Command:
Output Interrupt Control

Function Code:
03

Format:

Function:
Loads a 16-bit word into the interrupt control register with the information necessary for generating an interrupt, i.e., the interrupt level and which CP the interrupt is to be issued to. On interrupting, the CP channel number is returned on the address bus while the interrupt level is returned on the data bus.

Command:
Output Control
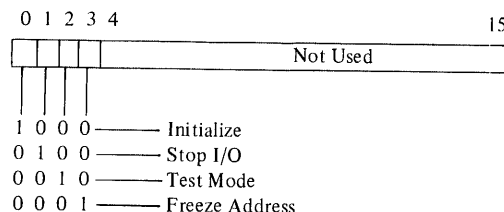
Function Code:
01

Format:

Function:
Loads a 16-bit control word into the referenced channel and will be accepted unconditionally regardless of any channel busy status. The channel may respond with a WAIT, but never with a NAK. The individual bits will cause the following specific actions to occur:

- Initialize
  - Causes the MDC to run its resident logic test
  - Clears all four MDC Device-Pacs
  - Clears the Bus Interface
  - Blocks Interrupts
  - Resets the Busy Condition
  - Operates on all channels of a MDC
  - Sets card reader attachment to ASCII mode

- Stop I/O
  - Resets Busy Condition
  - Causes Interrupt if enabled
  - Abruptly stops transfer from card reader
  - Updates status in MDC R/W memory
  - Does not affect other channels

- Freeze Address
  - Prevents the MDC from modifying its DMA address register during operation. The card reader operates normally in all respects except that the entire card is input to a single memory address.

- Test Mode
  - Refer to paragraph entitled "Test Mode"

Command:
Output Address and Range

Function Code:
09

Format:

```
0                                              23
 ┌────────────────────────────────────────────┐
 │              Address Transfer                │
 └────────────────────────────────────────────┘

     0                         15
      ┌─────────────────────────┐
      │      Range Transfer      │
      └─────────────────────────┘
```
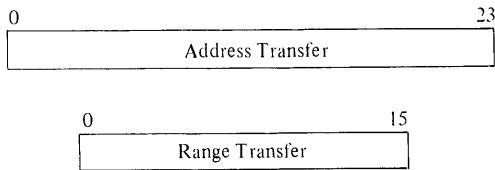
Function:

The IOLD command when executed by the processor creates two bus transfers to the MDC. The first is the 24-bit address transfer and the second is the 16-bit range transfer. To the MDC, these are two separate and distinct bus transfers with two separate and distinct function codes of 09 for the address transfer and 0D for the range transfer. The programmer need only specify the first function code and the processor hardware/firmware will automatically calculate the second function code (by adding 04 to it).

- Address Transfer — A 24 bit quantity transferred to the MDC to be used as the starting byte address of the data record in memory where the card data will be stored.

- Range Transfer — A 16 bit quantity transferred to the MDC to be used as the byte range count of the data record in memory where the card data will be stored. Range is specified as two's complement for the MDC and must be positive. Therefore, range is $1 \le r \le 2^{15}-1$. For the card reader, range should not be greater than the number sufficient to input a single card. If range is set less than that number, the MDC will input only the specified number of characters. If the range is set larger than that number, the MDC will terminate transfer at end of card rather than at the end of the range.

The range transfer includes the implicit command "Start IO" and causes the MDC to start reading a card and go busy.

Command:
Output Configuration

Function Code:
11

Format:

```
0                                              15
┌┬────────────────────────────────────────────┐
││                  Not Used                    │
└┴────────────────────────────────────────────┘
 └ 0 = ASCII Mode
   1 = Binary Mode
```
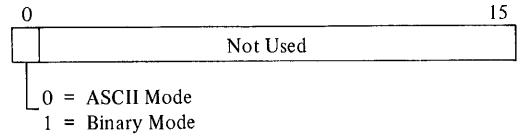
Function:
Outputs a word to determine in which of two modes the card reader will operate.

Input Commands

Command:
Input Interrupt Control

Function Code:
02

Format:

```
0                          9 10            15
 ┌──────────────────────────┬──────────────┐
 │    CP Channel Number      │  Interrupt   │
 │                           │    Level     │
 └──────────────────────────┴──────────────┘
```

Function:
Causes the channel to place the contents of its interrupt control register on the data bus.

Command:
Input Memory Byte Address

Function Code:
08

Format:

```
0                                              15
 ┌────────────────────────────────────────────┐
 │             Memory Address Bits              │
 │8 ──────────────────────────────────────▶23  │
 └────────────────────────────────────────────┘
```

Function:
Causes the channel to place the 16 least significant bits of its DMA address register on the data bus. The bits represent the memory address register bits 8-23.

NOTE: This command will violate memory protection.

Command:
Input Memory Module Address

Function Code:
0A

Format:

```
 0           7 8                    15
┌─────────────┬──────────────────────┐
│  Not Used   │ Memory Address Bits  │
│             │ 0 ──────────────────▶7│
└─────────────┴──────────────────────┘
```

Function:
Causes the channel to place the eight most significant bits of its DMA address register on the data bus. The bits represent memory address bits from 0 through 7 inclusive.

> NOTE: This command will violate memory protection.

Command:
Input Range

Function Code:
0C

Format:

```
 0                               15
┌─────────────────────────────────┐
│                                 │
└─────────────────────────────────┘
```

Function:
Causes the channel to place the contents of its range register on the data bus.

Command:
Input Configuration

Function Code:
10

Format:

```
 0                               15
┌─────────────────────────────────┐
│                                 │
└─────────────────────────────────┘
```

Function:
Causes the channel to place the contents of its configuration register on the data bus.

Command:
Input Status

Function Code:
18

Format:

```
 0                                                          15
┌──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┐
│0 │1 │2 │3 │4 │5 │6 │7 │8 │9 │10│11│12│13│14│15│
└──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┘
```

Bit labels:
0 – Device Ready
1 – Attention
2 – Data Service Rate Error
3 – Mark Sense Mode
4 – 40 Column Mode
5 – 51 Column Mode
6 – External Clock Track
7 – Read Check Error
8 – ASCII Code Error
9, 10, 11 – Not Used
12 – Corrected Memory Error
13 – Non-Existent Resource
14 – Bus Parity
15 – Uncorrectable Memory Error
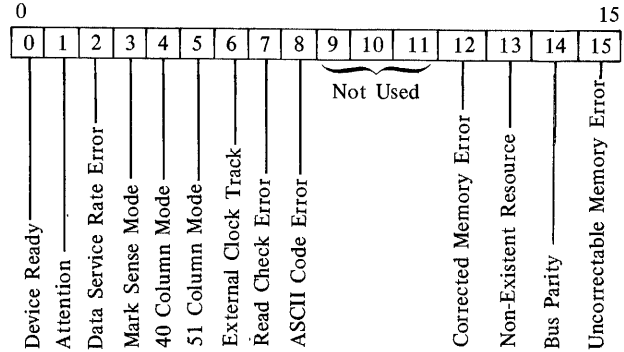
Function:
Causes the channel to place the contents of its status register on the bus. Also see Table 6-6.

Command:
Input Device ID

Function Code:
26

Format:

```
 0                       15
┌─────────────────────────┐
│                         │
└─────────────────────────┘
```
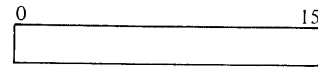
Function:
Causes the channel to place its device identification number (2008) on the bus.

Specifications

Types:

CRU9101 — 300 cpm, 80-column punched cards
CRU9102 — 300 cpm, 80-column punched cards, 40-and 80-column marked cards
CRU9103 — 500 cpm, 80-column punched cards
CRU9104 — 500 cpm, 80-column punched cards, 40- and 80-column marked cards
Input Hopper Capacity: 500 cards
Output Stacker Capacity: 500 cards
Programmed Operations: Read data from card

TABLE 6-6. STATUS BIT DEFINITIONS — CARD READER

Status Condition	Bit	Definition	Reset By
Device Ready	0	Card Reader on. Motor running. Input hopper not empty. Output hopper not full.	A change in condition.
Attention	1	Device ready condition has changed.	Read status word 1.
Data Service Rate Error	2	The MDC/CP/BUS have failed to meet the Card Reader speed and data has been lost.	Next IOLD command.
Mark Sense Mode	3	The Mark Sense/STD switch on the Card Reader is in the Mark Sense mode.	A change in switch position.
40 Column	4	The 40/80 Column switch on the Card Reader is in the 40 Col. position.	A change in switch position.
51 Column	5	The 51/80 column switch on the Card Reader is in the 51 Col. position.	A change in switch position.
External Clock Track	6	The Clock Track/Internal clock switch on the Card Reader is in the Clock Track position.	A change in switch position.
Read Check	7	The Card Reader failed to meet a light-dark check indicating possible device failure.	Next IOLD command.
ASCII Error	8	A pattern from card which does not translate to ASCII (in ASCII mode only). Data in error forced to all Ones.	Next IOLD command.
Corrected Memory Error	12	The Card Reader Device-Pac never reads memory and will never receive this indication from memory.	Next IOLD command.
Non Existent Resource	13	A NAK was received from memory. Indicates possible programming error.	Next IOLD command.
Bus Parity	14	Parity incorrect on bus transfer toward MDC.	Next IOLD command.
Noncorrectable Memory Error	15	The Card Reader Device-Pac never reads memory and will never receive this error indication from memory.	--

Device Interface: Each card reader requires its own Device-Pac (CRM9101)
Data Transfer Mode: Automatic translation via system software of Hollerith or binary to ASCII
Reading Technique: Photoelectric, column-by-column serially
Card Specification: Standard punched or mark cards, 7 3/8 in. x 3 1/2 in. (18,6cm x 8,9cm), 0.00770 in. (0,01956cm) thick; cards must be clean and free from excessive curl
Physical Dimensions: 13 1/2 in. (34,3cm) high, 19 1/4 in. (48,9cm) wide, 14 3/4 in. (37,5cm) deep
Weight: 35 lb (15,9k)
Required Input Power: 115 Vac ± 10%, 48 — 66 Hz, 175W

TELEPRINTERS

Two teleprinter console devices, Types TTU9101 (ASR-33) and TTU9102 (KSR-33), are available for Level 6 system console and I/O use (Figure 6-5). Similar in operation and specifications, they interface with the 6/30 Model processors by means of a single-board Multiple Device Controller (MDC9101), a Console Device-Pac (KCM9101), and a 50-foot cable. Up to four teleprinters can be connected to a single MDC.

Both teleprinter consoles print data from or transmit data to the central processor at the rate of ten characters per second. The TTU9101 can also read and punch paper tape at the same rate. The TTU9102 does not read or punch paper tape.
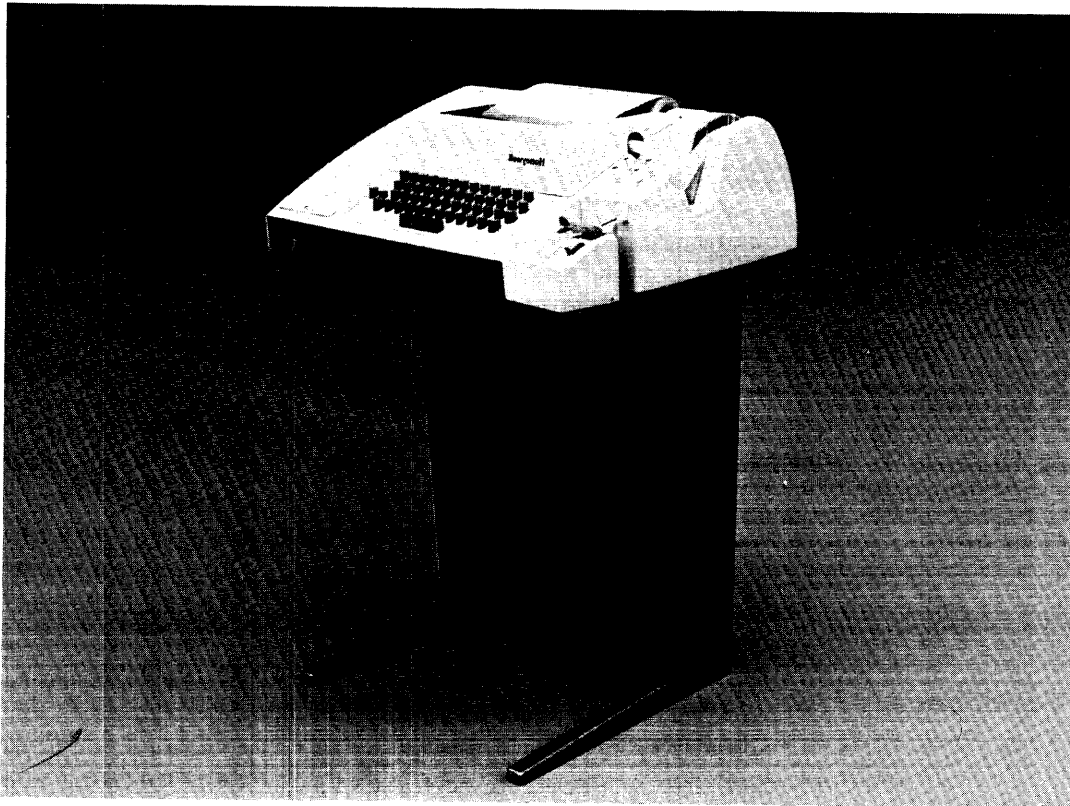
Figure 6-5. TTU9101 Teleprinter Console (ASR-33)

Features

- Printing and paper tape reading and punching in both online and offline modes (TTU9101)
- Online operation in full-duplex mode
- Test mode for easy maintenance

Operation

The teleprinter console control contains two eight-bit registers for full-duplex operation. Data transfers between the teleprinter console and the Level 6 processor are bit-parallel and under DMA (Direct Memory Access) control.

While waiting for the buffer to become ready, the computer is free to perform other operations. A program interrupt signals the central processor when further device servicing is required by the software.

Printer

The operations that the console printer can perform are:

- Print one line
- Space n lines (n ⩽ 15)
- Space n lines and print.

Spacing will be done before printing. The software has control over whether the MDC will send a control character (e.g., CR) to the printer at the end of range or not. The line length and the specific control character required at the end of the line are determined by the specific console device chosen.

A programmer may also do page printing, if desired, by outputting a sufficient range and inserting suitable control characters in the data stream.

Keyboard

The console keyboard may be used by the operator to input a message to a DMA block which had been previously set up by software. The range is typically set larger than the message which is to be entered. Software control exists over the type of character editing which is to be performed by the MDC.

- Define which character will terminate the operation, when entered.
- Define which character performs a backspace, when entered.
- Define which character will cause the preceding input message to be discarded.

- Define a visible escape character so that arbitrary constants may be entered through the keyboard.

Paper Tape Reader

Software must issue a specific control character to the reader to start it. A DMA operation is then set up to read the tape. The record on tape should be equal to or less than the DMA range. The Console can be set up by software to issue, under the following conditions, a control character to the reader to turn it off.

- End of range
- Specific character encountered on tape
- Break detected
- Stop I/O from software

The reader will respond to the following ASCII control codes:

DC1 or X-ON — Automatically turns reader on.
DC3 or X-OFF — Automatically turns reader off.
ENQ — Turns reader off.
EOT — Turns reader off.

NOTE: These characters must be sent via an output order to the TTY. The reader does not stop upon reading the control character.

Paper Tape Punch

Software must issue a specific control character to the punch to turn it on. A DMA operation is then set up and the contents of the DMA block are punched. Where the record to be punched is greater than the DMA range, software will set up a new DMA block at end of range. The Console can be set by software to issue a control character to the punch under certain conditions:

- End of Range
- Error from Memory
- Break Detected
- Stop I/O from Software

The specific control character is programmable and can be used, for example, to turn off the punch.

The punch will respond to the receipt of ASCII control codes as follows:

DC2 or TAPE — Turns the punch on
DC4 or TAPE — Turns the punch off.

When sending these control characters to the punch, the software must insure that they are both followed by at least one DEL; i.e.:

DC2, DEL — Turns punch on. These two characters *are not* punched. All subsequent characters are punched until the punch is turned off.

Data Format

The range of the data buffer in memory is expressed in bytes and is even or odd. The starting address may be on any byte boundary. Data read or written by the MDC is packed two bytes per word. In the case of an odd byte (which may be at the start or end of block), only the designated byte may be transferred. The Console is set (by software) to operate in either of two modes:

- 8 bit direct transcription, or
- 7 bit with even parity.

In case 7 bit mode is selected, the MDC generates the parity on output transfers and checks parity on input transfers. Figure 6-6 illustrates the bit designations. Bit designations relative to the holes in the paper tape are shown in Figure 6-7.

Instructions

Table 6-7 lists the I/O commands to which the MDC/teleprinter Device-Pac/teleprinters respond. A detailed description of each command follows.

NOTE: The instructions and programming information presented in this section (exclusive of paper tape operations) also pertains to users of the DKU9101 CRT Keyboard Console Unit and the TWU9101 Keyboard Typewriter Console.

Output Commands

Command:
Output Interrupt Control

Function Code:
03

Format:

0	9	10	15
CP Channel Number		Interrupt Level	

Function

Loads a 16-bit word into the interrupt control register with the information necessary for generating an interrupt, i.e., the interrupt level and which CP the interrupt is to be issued to.
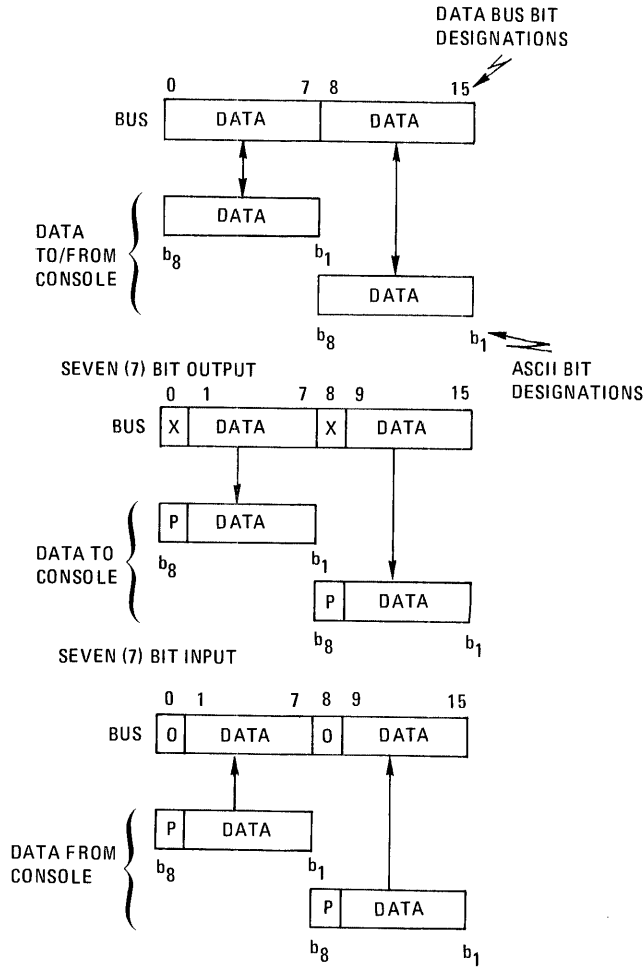
Figure 6-6. Bit Designations
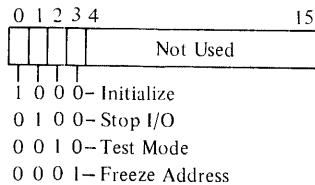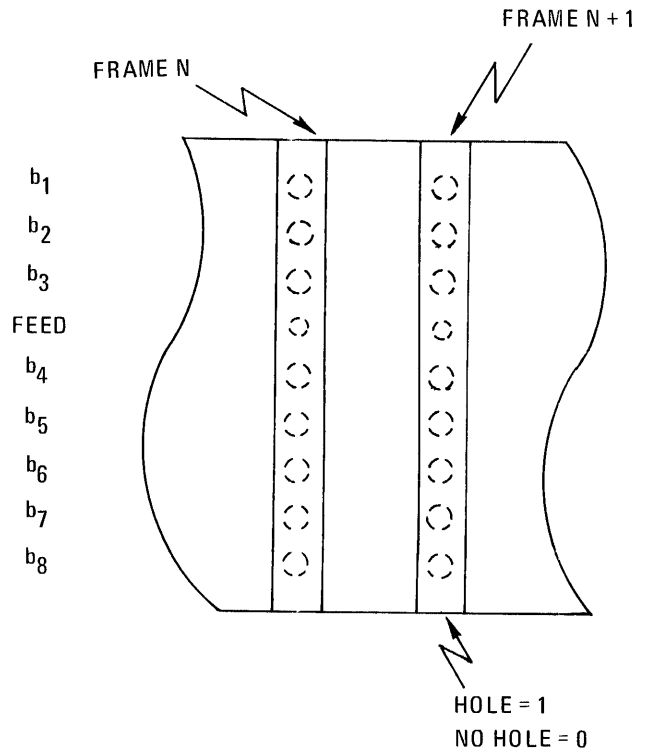
Figure 6-7. Bit Designations on Paper Tape

TABLE 6-7. TELEPRINTER COMMANDS

Type	Function Code	Command
Output	03	Output Interrupt Control
	01	Output Control
	09	Output Address and Range
		NOTE: The low order bit of this command specifies the direction of data transfer.
	11	Output Configuration Word A
	13	Output Configuration Word B
	07	Output Task
Input	02	Input Interrupt Control
	0C	Input Range (Residual)
	10	Input Configuration Word A
	12	Input Configuration Word B
	18	Input Status Word
	26	Input Device ID
	08	Input Memory Byte Address
	0A	Input Memory Module Address
	06	Input Task Word

Command:
Output Control

Function Code:
01

Format:

Function:
Loads a 16-bit control word into the referenced channel and will be accepted unconditionally regardless of any channel busy status. The channel may respond with a WAIT, but never with a NAK. The individual bits will cause the following specific action to occur:

• Initialize
   — Causes the MDC to run its resident logic test
   — Clears all MDC Device-Pacs
   — Operates on all channels of MDC
   — Makes all channels of MDC non-busy
   — Blocks interrupts

- Stop I/O
  - Makes channel non-busy (causes interrupt if enabled)
  - Does not affect other channels
  - Causes channel to terminate its I/O operation and update status

- Freeze Address
  - Prevents the MDC from modifying its DMA address register during operation. The console works normally in all respects except that the entire transfer takes place from the same memory location.

- Test Mode
  - See paragraph entitled "Test Mode."

Command:
Output Address and Range

Function Code:
09

Format:

```
0                                    23
+------------------------------------+
|         Address Transfer           |
+------------------------------------+
```

```
0                    15
+--------------------+
|   Range Transfer   |
+--------------------+
```

Function:
The IOLD command when executed by the processor creates two bus transfers to the MDC. The first is the 24-bit address transfer and the second is the 16-bit range transfer. To the MDC, these are two separate and distinct bus transfers with two separate and distinct function codes of 09 for the address transfer and OD for the range transfer. The programmer need only specify the first function code and the processor hardware/firmware will automatically calculate the second function code (by adding 04 to it).

- Address Transfer — A 24 bit quantity transferred to the MDC to be used as the starting byte address of the data record in memory which is to be transferred.

- Range Transfer — A 16 bit quantity transferred to the MDC to be used as the byte range count of the data record in memory which is to be transferred. Range is specified as a two's complement integer which must be positive for the MDC. Therefore, for the MDC, Range is:

$$1 \leqslant r \leqslant 2^{15} - 1$$

The range transfer includes an implicit start I/O command. When received by the MDC it causes the addressed channel to go busy and perform the operation indicated by the previously supplied I/O commands.

The LSB of the channel number (address bus bit 17) designates direction for this particular DMA transfer. Output transfers have the LSB of the channel number = 1. Input transfers have the LSB = 0.

Command:
Output Configuration Word A
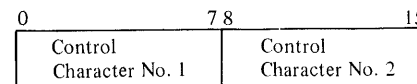
Function Code:
11

Format:

```
0                7 8               15
+----------------+-----------------+
|   Control      |   Control       |
| Character No. 1| Character No. 2 |
+----------------+-----------------+
```

Function:
Outputs a word consisting of two control characters necessary during the execution of an input command.

- Control Character #1, when detected, will cause the console to perform a backspace, (i.e., the last character entered is eliminated from the input buffer). This is applicable to keyboard operations only.
- Control Character #2, when detected, will cause the console to terminate the input order, post the appropriate status bit and send an interrupt (if interrupt is allowed).

Following an initialize, control characters 1 and 2 will be reset to zero.

Command:
Output Configuration Word B
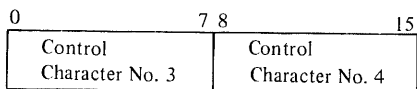
Function Code:
13

Format:

0	7	8	15
Control Character No. 3		Control Character No. 4	

Function:
Outputs a word consisting of two control characters necessary during the execution of an input or output command.

- Control character #3 is used differently as a function of the command type. During the execution of an input command type, detection of control character #3 will cause the console to terminate the input order. In addition, upon termination of an input order (either normally or abnormally) control character #3 will be sent to the console to position the carriage to its home position or stop the tape reader.
  During the execution of an output command type, control character #3 will be sent to the console, if so specified in the command, with the purpose of positioning the carriage to its home position or stopping the paper tape punch.

- Control character #4 applies to input operations only. When received from the console, this character is discarded by the MDC and the character immediately following is input to memory regardless of its value. Control character #4 is used as an escape character so that the operator can input a character that was equal to CC1, CC2 or CC3 without causing the actions described for them. If control character #4 is set to zero, which it

is following an initialize, none of the escape actions described here will occur.

Command:
Output Task

Function Code:
07

Format:
For an *output* operation (print or punch) the task word has the following format:

0	6	7	8	9	10	11	12	15
Not Used	B/NB	RFU		CR/NCR	7/8	RFU		
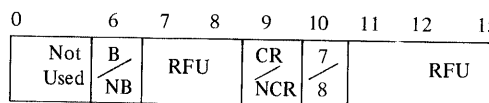
Bit 10 - Specifies the character width. 0 = 7 bit with even parity. The Device-Pac will take a byte from memory and alter its high order bit (if necessary) in order to obtain an even number of 1 bits. The byte is then sent to the TTY. 1 = 8 bit direct transcription. The Device-Pac takes the byte from main memory and sends it to the TTY with no modification.

Bit 9 - Specifies whether or not control character #3 is to be sent to the TTY when the range equals zero.

0 = Send CC #3
1 = Do not send CC #3

Bit 6 - Specifies the required console action when a break is detected during an output operation. 0 = post break detected but continue current operation until its completion. 1 = post break detected and stop immediately current operation.

For an *input* operation (keyboard or paper tape read), the task word has the following format:

```
0    5   6   7   8   9   10          15
┌──────┬──┬──┬──┬──┬────┬──┬───────────┐
│ Not  │0 │R │E │0 │CR  │7 │           │
│      │╱ │F │╱ │╱ │╱   │╱ │ Not Used  │
│ Used │1 │U │NE│1 │NCR │8 │           │
└──────┴──┴──┴──┴──┴────┴──┴───────────┘
```
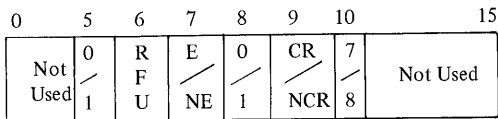
Bit 10 specifies the character width.

0 - 7 bit with even parity. The Device-Pac will insure that the byte received from the TTY contains an even number of 1 bits. In addition when storing the byte in main memory, it will set the high order bit to zero.

1 = 8 bit direct transcription. The Device-Pac performs no checks on the byte received from the TTY and stores all 8 bits in the main memory.

Bit 9 specifies whether or not control character #3 is to be sent to TTY when the range equals zero.

0 = Send CC #3
1 = Do not send CC # 3

Bit 8

0 = Check for control characters on input
1 = Do not check for control characters on input

Bit 7 specifies whether or not echoing is required.

0 = No echo
1 = Echo character

Bit 5

0 = Append attention character
1 = Discard attention character

Function:

Outputs a word which determines the specific action to be performed. Bit interpretations differ for output and input operations. When this word is received by the MDC it is stored. The next IOLD command which is issued specifies the direction and, therefore, the interpretation. The task word will remain stored in the Device-Pac until a new task word is issued or initialize occurs.

An input command is used to either accept a message from the keyboard or read a block (or part of it) from a paper tape mounted on the paper tape reader. A detailed description of the read keyboard or paper tape operation is given in the section entitled "Programming Considerations."

An output command is used to perform one of the following operations:

- Print/display a message to the operator
- Format the printer/display
- Start a paper tape punch
- Punch paper tape
- Start a paper tape reader.

Input Commands

Command:
Input Interrupt Control
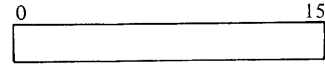
Function Code:
02

Format:

```
0                          15
┌──────────────────────────┐
│                          │
└──────────────────────────┘
```

Function:
Causes the channel to place the contents of its interrupt control register on the data bus.

Command:
Input Range

Function Code:
0C

Format:

```
0                          15
┌──────────────────────────┐
│                          │
└──────────────────────────┘
```
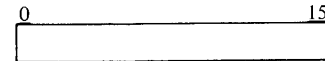
Function:
Causes the channel to place the contents of its channel register on the data bus.

Command:
Input Configuration Word A

Function Code:
10

Format:

```
0                          15
┌──────────────────────────┐
│                          │
└──────────────────────────┘
```
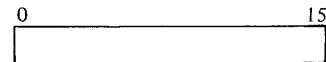
Function:
Causes the channel to place the contents of its configuration word A register on the data bus.

Command:
Input Configuration Word B

Function Code:
12
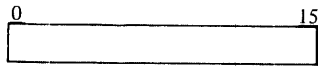
Format:

Function:
Causes the channel to place the contents of its configuration word B register on the data bus.

Command:
Input Status Word

Function Code:
18

Format:
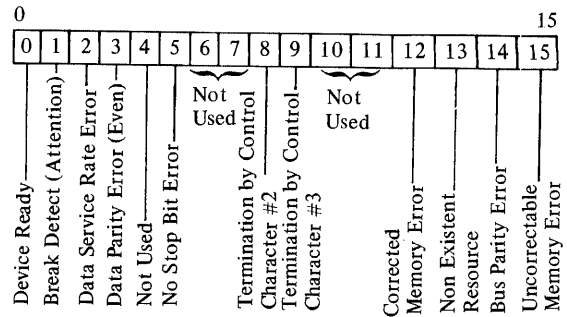
Function:
Causes the channel to place the contents of the status register on the bus. See also Table 6-8.

TABLE 6-8. STATUS BIT DEFINITIONS – TELEPRINTER

Status Condition	Bit	Definition	Reset By
Device Ready	0	In current loop connections, this indicates that the console is connected by the presence of the output current when the Device-Pac is not busy, i.e., not sending data to the console. In EIA connections, this indicates Data Terminal Ready for direct connections or Carrier Detect for data set connection.	Change of status
Break Detect (Attention)	1	Operator pressed Break key. Bit 6 of the task word specifies the MDC action to be taken when this is received.	Initialize or status word fetch
Data Service Rate Error	2	While receiving, the MDC failed to take a character from the Device-Pac before the next character arrived.	Same as preceding bit
Data Parity Error (even)	3	Device-Pac detected a data parity error. This is only applicable if the task word was set to specify 7 bit mode (Bit 10 = 0).	Same as preceding bit
No Stop Bit Error	5	A character was received from the console without a stop bit.	Same as preceding bit
Termination by Control Character #2	8	Control character #2 was detected in the input stream and caused a termination.	Next IOLD or initialize
Termination by Control Character #3	9	Control character #3 was detected in the input stream and caused a termination.	Same as preceding bit
Corrected Memory Error	12	The data read from memory was accompanied by a signal indicating an error was corrected.	Same as preceding bit
Non Existent Resource	13	A reference was made to a memory address that did not exist.	Same as preceding bit
Bus Parity Error	14	The Device-Pac detected bad bus parity on a transfer toward the MDC.	Input status or initialize
Uncorrectable Memory Error	15	The data read from memory was accompanied by a signal indicating an error existed that the memory could not correct.	Next IOLD or initialize

Command:
Input Device ID

Function Code:
26

Format:

```
0                    15
┌──────────────────────┐
│                      │
└──────────────────────┘
```

Function:
Causes the channel to place its device identification number (2018 for the TTU9102; 2019 for the TTU9101; 2020 for the DKU9101) on the bus.

Command:
Input Memory Byte Address
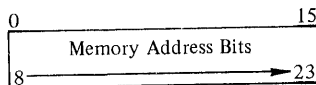
Function Code:
08

Format:

```
0                         15
  ┌──────────────────────┐
  │  Memory Address Bits  │
  │8──────────────────▶23│
  └──────────────────────┘
```

Function:
Causes the channel to place the 16 least significant bits of its DMA address register on the data bus. The bits represent the memory address register bits 8-23.

  NOTE: This command will violate memory protection.

Command:
Input Memory Module Address

Function Code:
0A

Format:

```
0             7 8           15
  ┌───────────┬──────────────┐
  │           │Memory Address Bits│
  │ Not Used  │              │
  │           │0──────────▶7│
  └───────────┴──────────────┘
```
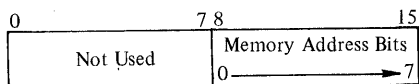
Function:
Causes the channel to place the eight most significant bits of its DMA address register on the data bus. The bits represent memory address bits from 0 through 7 inclusive.

  NOTE: This command will violate memory protection.

Command:
Input Task Word

Function Code:
06

Format:

```
0                    15
┌──────────────────────┐
│                      │
└──────────────────────┘
```

Function:
Causes the channel to place the contents of its task word register on the bus.

Programming Considerations – Console
The operations required by the software to control the console are the following:

- Load Configuration
- Read Keyboard (i.e., read a message entered by the operator through the keyboard)
- Print/Display (i.e., print or display a message to the operator on the printer
- Read Status
- Stop I/O (i.e., stop the I/O operation currently in progress)
- Attention (i.e., react to the detection of an operator generated Break request).

Load Console Configuration Operation
Prior to executing a read or print/display operation, the software must preset the TTY by loading it with the appropriate configuration word(s) to insure proper operation execution.

The configuration information need be loaded only once before a series of console operations and will remain unchanged until a paper tape operation is performed. Thus any console operations which follow at least one paper tape operation must be preceded by a load configuration operation.

Two commands are available to load the console configuration information, they are:

- Output Configuration Word A
- Output Configuration Word B

The contents of the configuration words should be as shown in Table 6-9. The console control characters and character set is shown in Table 6-10.

TABLE 6-9. CONTENTS OF CONFIGURATION WORDS – CONSOLE

Operation Performed	Configuration Word A Consists of 2 Bytes		Configuration Word B Consists of 2 Bytes	
	Set Control Character #1 To:	Set Control Character #2 To:	Set Control Character #3 To:	Set Control Character #4 To:
Read	∧ (Note 1)	@ (Note 1)	CR (Note 2)	\ (Note 1)
Print/Display	Not Used	Not Used	CR (Note 2)	Not Used Set to 00

NOTES:

1. This specific character is chosen by software convention, however other values are permitted.

2. This specific character is required by the ASR TTY peripheral. Any other character configured here would be output to the device and would cause an action determined by the specific peripheral used.

TABLE 6-10. CONSOLE CODE SET

b7 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
Bits b4	b3	b2	b1*	Column → Row ↓	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	–	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	∧	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

*b_1 is low order bit

All characters in these two rows + SP (space) and DEL (delete) are non-printing.

"Fold-over Printing" means that lower case characters received by model 33's are actually printed as their upper case equivalent. Codes shown in Columns 6 & 7 of the chart "fold-over" into Columns 4 & 5 respectively, (except for "DEL").

Read Keyboard Operation

A read operation is initiated by the software to allow an operator to generate a message via the keyboard. The following commands must be issued by the software to the TTY to initiate the read operation:

- Output Task
- Output Address and Range (IOLD)

The sequence in which the above listed commands must be issued is as shown, otherwise unspecified results occur. However, if a series of Read Keyboard Operations is to be performed, then the Output Task command need be sent only once. All subsequent Read Operations need only the Output Address and range command. Typically, the software will initiate a read operation with interrupt allowed and set the range to 72 characters. Thus it will be interrupted only after the receipt of a complete message.

If operating in non-interrupt mode then the software will have to periodically issue an Input Status Word command and test the I-bit of the CP I-register. This bit will reflect the state of the attachment i.e., busy or not.

The range should normally be set to 72, but if set to less, then upon detection of range equal to zero, the attachment will automatically terminate the order and perform a carriage return.

A Read operation is initiated upon receipt of the Output Address and Range command. The channel number will have its lower bit set to zero. It should be set as follows:

Task Word Used to Read a Message	0 5	6	7	8	9	10	15
	RFU	0⟋1	R F U	E⟋NE	0⟋1	CR⟋NCR	7⟋8	Not Used

BIT 5 - Set to 0 to append attention character or set to 1 to discard it.

BIT 7 - Set to 1 or echo all characters received from the keyboard to the printer. (Recommended rather than required.)

BIT 8 - Set to 0 to check for control characters on input or set 1 to not check for control characters.

BIT 9 - Set to 0 or send control character #3 to the TTY when the range equals zero.

BIT 10 - Set to 0 or 7 bit with even parity.

The functions performed during execution of the read operation are as follows:

- Accept the characters typed by the operator, store them in the main memory buffer, and print them on the printer.

- Edit the text in conjunction with the software. Specifically, upon detection of the control character.

∧ — Eliminate the last valid entered character from the main memory buffer by updating the range and address pointers. (The deleted data character is not erased from the main memory buffer but will be overwritten by the next data character, if any.)

@ — Inform the software that the operator desires to cancel the line just entered. The software will then re-issue the read operation.

\ — Discard the control character and input the following character regardless of its value. This is an escape mode which allows the input from the keyboard of a character which has a value equal to one of the other three control characters without the usual action being taken.

- Position the carriage/cursor at the home position upon termination of the read operation. Then set the attachment in the unbusy state and send interrupt if so required.

Print/Display Operation

A print/display operation is initiated by the software to output a message to the operator. The following commands must be issued by the software to the TTY attachment to initiate the output operation.

- Output Task
- Output Address and Range (IOLD)

The sequence in which the above listed commands must be issued is as shown, otherwise unspecified results will occur. However, if a series of similar Print/Display Operations is to be performed, then the Output Task command need be sent only once. All subsequent Print/Display operations need only the Output Address and Range command.

Typically, the software will initiate an output operation with interrupt allowed and thus will not be interrupted until the entire message has been printed/displayed.

If operating in non-interrupt mode then the software will have to periodically issue an Interrupt Status Word 1 command and test the I-bit of the CP I-register. This bit will reflect the state of the attachment, i.e., busy or not.

An output operation is initiated upon receipt of the Output Address and Range command. The channel number will have its lower order bit set to one. The task word should be set as follows:

Task Word Used
To Print/Display
a Message

0	6	7	8	9	10	11	12	15
RFU	B/NB	∅	∅	CR/NCR	7/8	RFU		

BIT 6 - Optional, can
specify either; just log
break condition or stop
immediately the output
operation.

BIT 9 - Optional, can specify
carriage return/cursor home
or not.

BIT 10 - Set to 0 or
seven bit with even
parity.

The functions performed during the execution of an output operation can be one or more of the following in the order shown:

- Space 0-15 lines
- Print a message or do not print
- Perform a carriage return or not.

When used in this mode, which is one line of print per IOLD, the TTY automatically performs the carriage return if so requested. If it is desired to print more than one line, the text will have to contain: CR, LF, DEL, DEL every 72 characters or less (one line length). Failure to do this will result in loss of the data characters beyond character number 72.

Console Read Status Operation

A Read Status Operation is initiated by the software in order to determine the outcome of an input or output operation or upon receipt of an unsolicited (Attention) interrupt. The following commands are issued by the software to the TTY:

- After a Read Keyboard Operation
  - Input status
  - Input range
- After a Print Operation
  - Input status
- Upon receipt of an unsolicited (Attention) interrupt
  - Input Status

Following a read keyboard operation, the software must retrieve the residual range in order to determine the length of the input message.

Typically, the software will be interrupt-driven and thus will perform a Read Status Operation only upon receipt of an interrupt.

If operating in non-interrupt mode then the software will perform a Read Status Operation following the execution of an input or output operation in order to determine its completion and outcome.

Console Stop I/O Operation

A Stop I/O Operation is initiated by the software to terminate gracefully an outstanding input or output operation. It is issued via an Output Control command having its bit 1 set to a one. Assuming no hardware faults in the controller, it will terminate the current order and enter the non-busy state. The console will also send an interrupt, if allowed.

Although the Stop I/O can be issued to terminate both input and output operations, it is expected that it will be used mainly to terminate outstanding read keyboard operations. This will result in those cases when no operator or response is detected following the expiration of a software controlled elapsed time.

Attention

Attention is the mechanism used by the operator to establish a dialogue with the system software. It is invoked by the operator, by pressing BREAK key on the keyboard.

Typical usages of this mechanism are:

- To make an inquiry
- To answer a question
- To terminate an output operation
- To direct the system software.

The functions performed by the attachment upon detection of an Attention are a function of the Device-Pac state :

- For Device-Pac Ready (not busy)
  - Store the Attention character in the MDC R/W memory
  - Send an interrupt to the software, if so allowed
  - Append the Attention character to the beginning of the next input message, if so requested, and echo to the console as verification to the operator.
- For Device-Pac Busy performing output
  - Store the Attention character in MDC R/W memory
  - If character is a break, check bit 6 of task word, terminate output and interrupt (bit 6 = 1)
  - Otherwise, just set Attention status and wait for normal termination of output.

- Attention does not pertain to input operations.

The reaction of the system software to an Attention will be:

- Output some sort of an acknowledgement message on the printer or display (e.g., a question mark)
- Issue a read keyboard command to accept the operator's message or command.

The Device-Pac will guarantee that only one Attention interrupt will result for every depression of a key.

Programming Considerations — Paper Tape

The operations required by the software to control the paper tape reader and punch are the following:

- Load Configuration
- Read Paper Tape
- Punch Paper Tape
- Read Status
- Stop I/O

Load Paper Tape Configuration Operation

Prior to executing a paper tape read or punch operation, the software must preset the TTY Device-Pac by loading it with the appropriate configuration word(s) to insure proper operation execution.

The configuration information need be loaded only once before a series of paper tape operations and will remain unchanged until a console operation is performed. Thus any paper tape operations which follow at least one console operation must be preceded by a load configuration operation.

Two commands are available to load the paper tape configuration information. They are:

- Output Configuration Word A
- Output Configuration Word B

The contents of the configuration words should be as shown in Table 6-11.

The specific characters in Table 6-11 are required by the TTU9101. Any other character configured here would be output to the device and would cause an action determined by the specific peripheral used.

Read Paper Tape Operation

A read operation is initiated by the software to read either one entire tape block or portion of a tape block. The following commands must be issued by the software to the TTY to initiate the read operation:

1. First the reader must be started via an output command sequence which sends one X-ON control character to the reader:
   a. Output Task and
   b. Output Address and Range (IOLD).
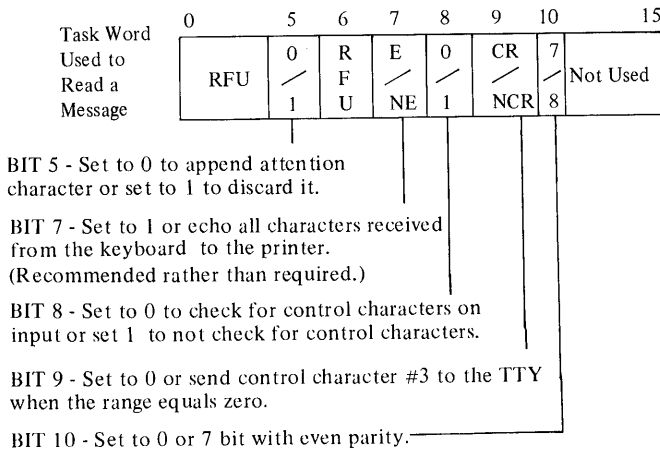2. Then the read order itself is issued via an input command sequence:
   a. Output Task and
   b. Output Address and Range (IOLD).

The sequence in which the above commands must be issued is as shown, otherwise unspecified results will occur. In addition, as soon as the first command sequence (that starts the reader) is completed, the second command sequence must be initiated to ensure no loss of information. The time between the two sequences should be less than two character frames (approximately 180 msec.).

Typically, the software will initiate a read operation with interrupt allowed and read one entire block. Thus it will be interrupted twice:

- After starting the reader and
- After one entire block has been read and the tape is stopped in the inter block gap.

TABLE 6-11. CONTENTS OF CONFIGURATION WORDS — PAPER TAPE

Operation Performed	Configuration Word A Consists of 2 Bytes		Configuration Word B Consists of 2 Bytes	
	Set Control Character #1 To:	Set Control Character #2 To:	Set Control Character #3 To:	Set Control Character #4 To:
Read	TAPE	TAPE	X off	Not Used Set to 00
Punch	Not Used	Not Used	TAPE	Not Used Set to 00

If operating in non-interrupt mode, then the software will have to periodically issue an Input Status Word command and test the I-bit of the CP I-register, to determine whether or not the attachment is still busy.

In addition, if the software reads a block in 2 or more segments, the reader is not capable of stopping between tape frames. Thus, the software must initiate a new read operation in less than one character time (approximately 90 msec.) or else data will be lost.

A read operation is initiated by starting the reader via an output sequence. It is initiated upon receipt of the Output Address and Range command issued to the output channel (lower order bit of channel number will be set to 1). It should be set as follows:

	0	6	7	8	9	10	11	12	15
Task Word Used to Start the Paper Tape Reader	Not Used	0/8	0	0	CR/NCR	7/8	0	0 0 0 0	

Bit 6 — Set to zero or log break if detected, but do not terminate output.

Bit 9 - Set to 1 or do not send control character #3 to TTY

Bit 10 - Set to 1 or 8 bit transfer to TTY

Bit 12 - 15 - Set to 0
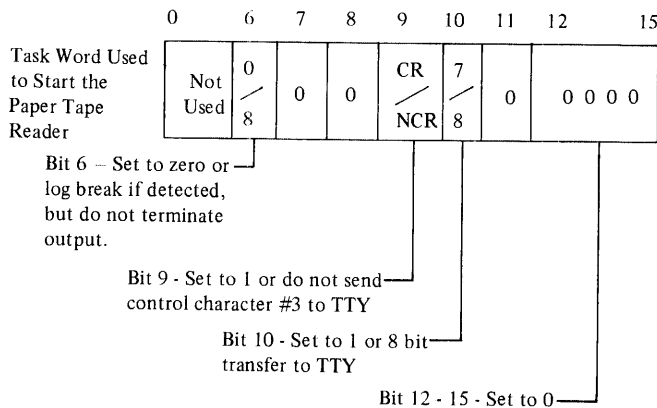
The Output Address and Range command should point to one X-ON control character (HEX code = 11).

The functions performed during the start reader sequence are:

● Send one X-ON character to TTY (software)
● If operation terminates successfully then set the TTY to the unbusy state and send interrupt, if so required.
● If operation terminates because either a Stop I/O, Break or error condition was detected, then STOP the reader by sending it Control Character #3 (set to X=OFF).

NOTE: When performing a read operation, the configuration parameters are set to the read state although both an output and input sequence are executed.

Next a read sequence must be issued. The read operation is initiated upon receipt of the Output Address and Range command issued to the input channel. The channel number will have its lower order bit set to zero. It should be set as follows:

	0	5	6	7	8	9	10	15
Task Word Used to Read a Paper Tape Block	RFU	1/0	0	E/NE	R/FU	CR/NCR	7/8	RFU

Bit 5 – Set to one or discard the attention character.

Bit 7 - Optional, although it is expected that most of the time Bit 7 = 0 or no echo required.

Bit 9 - Set to 1 or do not send control character #3 to the TTY when the range equals zero.

Bit 10 - Optional, depends on data type being read.
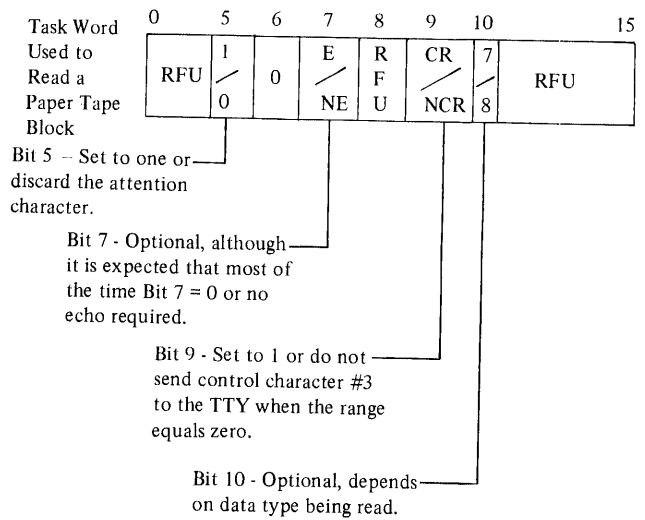
The functions performed during the read sequence are:

● Accept the characters read by the reader and store them in the main memory buffer.
● The data read is also printed, if so specified.
● If read operation terminates because range = 0, then do not stop reader but set the attachment to the unbusy state and send interrupt, if so required.
● If read operation terminates because a control character #2 (set to TAPE) or control character #3 (set to X-OFF) is detected, then stop reader by sending it control character #3. Then set the TTY to the unbusy state and send interrupt, if so required.

Punch Paper Tape Operation

A punch operation is initiated by the software to generate either one entire tape block or portion of a tape block. The following commands must be issued by the software to the TTY to initiate the output operation.
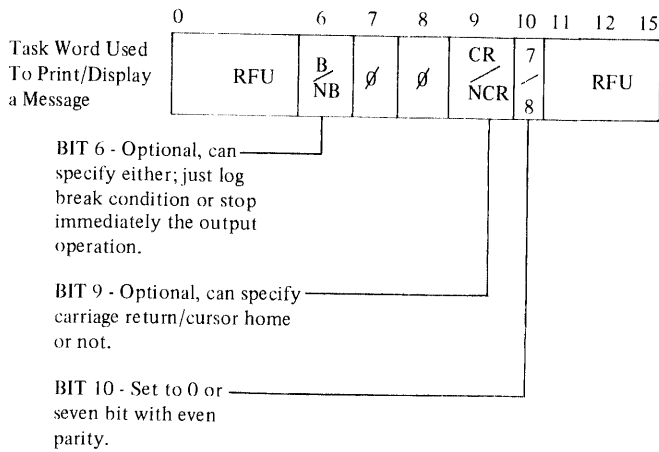
● Output Task
● Output Address and Range (IOLD)

The sequence in which the above listed commands must be issued is as shown otherwise unspecified results will occur. However, if a series of paper tape punch operations is to be performed, then the output task command need be sent only once. All subsequent punch operations need only the output address and range command.

Typically, the software will initiate a punch operation with interrupt allowed and punch one entire block. Thus it will be interrupted only after the entire block has been punched.

If operating in non-interrupt mode, then the software will have to periodically issue an Input Status Word command and test the I-bit of the CP I-register to determine whether or not the attachment is still busy.

If the software punches a block in 2 or more segments, the punch will stay on between segments and thus no console print/display operation should be initiated until the punch is stopped (else the data printed/displayed will also appear on the tape).

The punch operation is initiated upon receipt of the Output Address and Range command. The channel number will have its lower order bit set to one. It should be set as follows:

	0	5	6	7	8	9	10	11	15
Task Word Used to Punch Paper Tape	MBZ		B / NB	M B Z	0	CR / NCR	7 / 8	0	0000

·Bit 6 - Optional, can specify either just log break condition or stop immediately the output operation.

Bit 9 - Optional if punching an entire block then set Bit 9 = 0 i.e., send control character #3 (TAPE OFF) to TTY when the range = 0.

If punching only a segment then set Bit 9 = 1, i.e., do not send control character #3 to TTY when the range = 0.

Bit 10 - Optional, depends on data type being punched.

Bits 12 - 15 Set to 0

The functions performed during the Punch operation are:

● Start the punch. This is a software function and requires that two control characters (TAPE, DEL) be issued to the TTY. They are expected to normally be the first two characters in the punch buffer or possibly issued separately.
● Punch the block or a segment of it.
● Stop the punch if so specified after a normal termination. Then set the attachment to the unbusy state and send it an interrupt if so required.
● Stop the punch if either a Stop I/O or Break is detected. Then set the attachment to the unbusy state and send an interrupt if so required.

Paper Tape Read Status Operations

A Read Status Operation is initiated by the software in order to determine the outcome of an input or output operation. The Input Status Word command is issued by the software to the TTY.

Typically, the software will be interrupt driven and thus, will perform a Read Status operation only upon receipt of an interrupt.

If operating in non-interrupt mode, then the software will perform a Read Status operation following the execution of an input or output operation in order to determine its completion and outcome.

Paper Tape Stop I/O Operation

A Stop I/O Operation can be initiated by the software to terminate gracefully an outstanding input or output operation. It is issued via an Output Control command having its bit 1 set to a one. Assuming no hardware faults in the attachment, it will terminate the current order and enter the non-busy state. The attachment will also generate an interrupt if allowed.

It is not expected that Stop I/O operations will be used to stop paper tape operations. Nevertheless there might be situations caused by operator mistakes, (i.e., a paper tape is to be read, but it was not mounted) where the Stop I/O operation might be required.

Specifications

Printer
    Feed: Friction
    Paper Capacity: 8 1/2-inch (21.59cm) wide, 5-inch (12.70cm) diameter roll
    Print Speed: 10 characters per second
    Character Density:
        Horizontal — 10 characters per inch, 72 characters per line
        Vertical — 3 or 6 lines per inch
Punch (TTU9101)
    Tape: 1-inch wide, 8-level, paper or mylar-paper combination
    Tape Roll Capacity: 855-foot (260.6m) roll
    Punch Speed: 10 characters per second (feed and punch)
    Character Density: 10 characters per inch
Reader (TTU9101)
    Tape: 1-inch wide, 8-level, paper or mylar paper combination
    Read Speed: 10 characters per second
    Character Density: 10 characters per inch
EIA Interface
    Asynchronous data transfer with one or two stop bits; 110 baud operation

Device Interface

Each teleprinter console requires its own Console Device-Pac (KCM9101)

Physical Dimensions

TTU9101 (ASR-33): With pedestal — 32 7/8 in. (83.48cm) high, 22 in. (55.88cm) wide, 18 1/2 in. (46.99cm) deep; weight 56 lb. (25.37 kg)

TTU9102 (KSR-33): With pedestal — 32 7/8 in. (83.48 cm) high, 18 5/8 in (47.32 cm) wide, 18 1/2 in. (46.99 cm) deep; weight 52 lb. (23.56 kg)

Required Input Power: 115 VAC 10%, 48—66 Hz, 128W.

CRT KEYBOARD CONSOLE

The DKU9101 CRT Keyboard Console Unit permits conversational message transfer, status display, and operator control of any 6/30 Model system to which it is attached (Figure 6-8). Utilizing the latest in computer technology, it features a high level of reliability and yet maintains a relatively low price.

The DKU9101 consists of a CRT display unit with a detachable keyboard unit permitting flexibility of operation and placement. The CRT interfaces with the Level 6 processor by means of a single-board Multiple Device Controller (MDC9101) and a CRT Device-Pac (KCM9101).

Features

- Bottom line entry display with roll-up line feed
- Displays 960 positions on 12 lines of 80 positions each
- Displays 64 distinct characters including space plus audible alarm
- Keyboard has 60 encoded keys and N-key roll-over
- Keyboard can generate 128 ASCII codes using SHIFT, UNSHIFT and CONTROL keys
- BREAK, ESCAPE, DELETE, and CLEAR keys provide flexibility
- 60 mA current-loop interface or Bell 103A modem compatibility
- Two-way simultaneous or two-way alternate transmission
- Keyboard input displayable when received or upon transmission
- Two-way audible alarm

Keyboard

The console keyboard utilizes solid-state, high-reliability switches as keys. The keyboard permits the entry of variable data and program parameters. The 60 keys can generate 128 characters of the ASCII code set. The characters include 26 alphabetic, 10 numeric, and 32 special symbols.
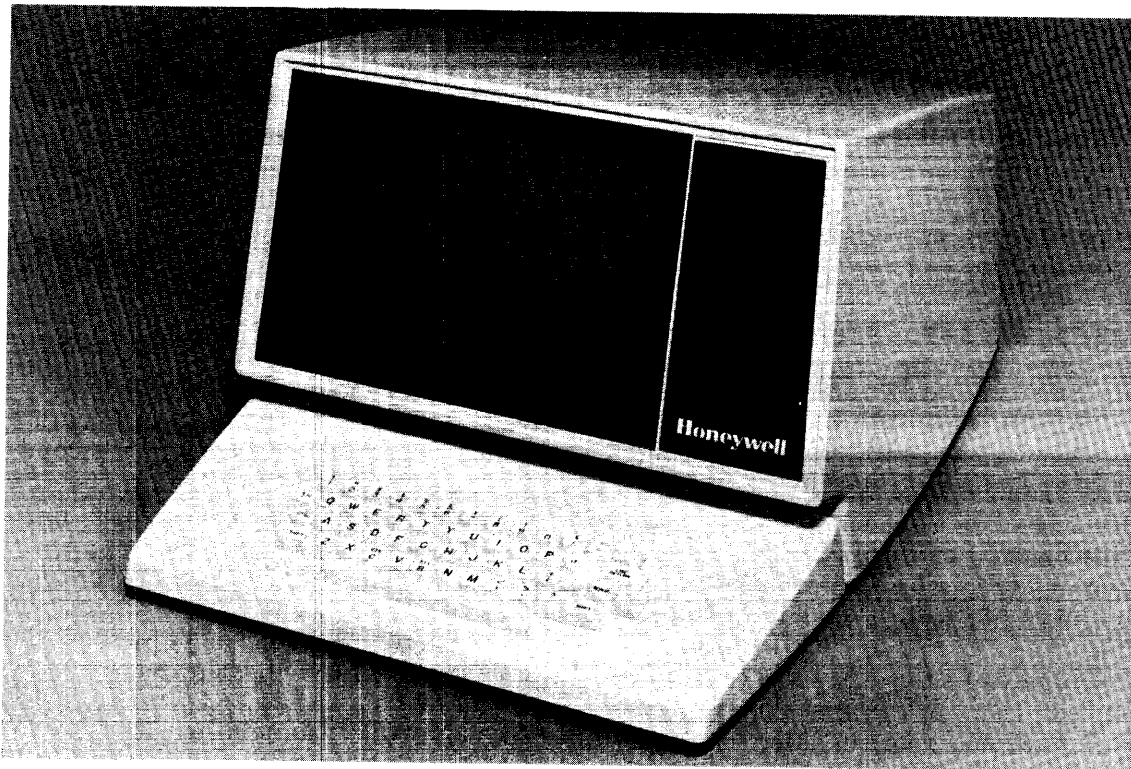
Figure 6-8. DKU9101 CRT Keyboard Console

Also included are 12 control keys. See Figure 6-9.

A special entry marker (cursor) appears on the console display screen to indicate the location of the next character to be displayed. The DKU9101 uses the "bottom line entry" approach for the display. The cursor moves only on the bottom line of the display. The bottom line display operates just like the print line of a journal roll, i.e., a line feed causes the entire display page (including the bottom line) to move up one line, leaving the new bottom line blank, or clear. A line return causes the cursor to move to the left margin first display position.

Display Screen

Manually entered data and processor-generated inquiries and responses are displayed on a 12-inch cathode ray tube. With a display of up to 960 characters (12 lines, 80 characters per line) and a 60 frames-per-second refresh rate, the display projects clear, bright, easily read information. The operator has access to all character positions within the bottom line.

Two-Way Audible Alarm

An operator-attention alarm sounds whenever the console receives a BEL code or when a character is displayed in the 75th character (or column) position.

Options

- DKU9102 – 95 character, upper and lower case display capability
- DFK9101 – Non-reflective faceplate

Operational Enhancements

Nondestructive cursor movement, backward and forward, a step at a time within the bottom line provides for applications enhancement. Clearing or erasing of the entire CRT screen via single key depression is also included to enhance operation.

These capabilities are inherent and may be enabled when desired. Additionally, the transmission rate is variable by steps between 75-9600 bps. Character size may include one or two stop bits as well as a choice for a parity bit to be odd, even or not needed. An extension 4-wire RS232C voltage level interface port is provided to accommodate an auxiliary device, e.g., a serial printer.

Instructions

The instructions and programming information presented for the teleprinters (excluding paper tape operations) is also applicable for the CRT Keyboard Console.

Specifications

Keyboard
TTY layout; 60 keys/128 character ASCII code set; N key rollover
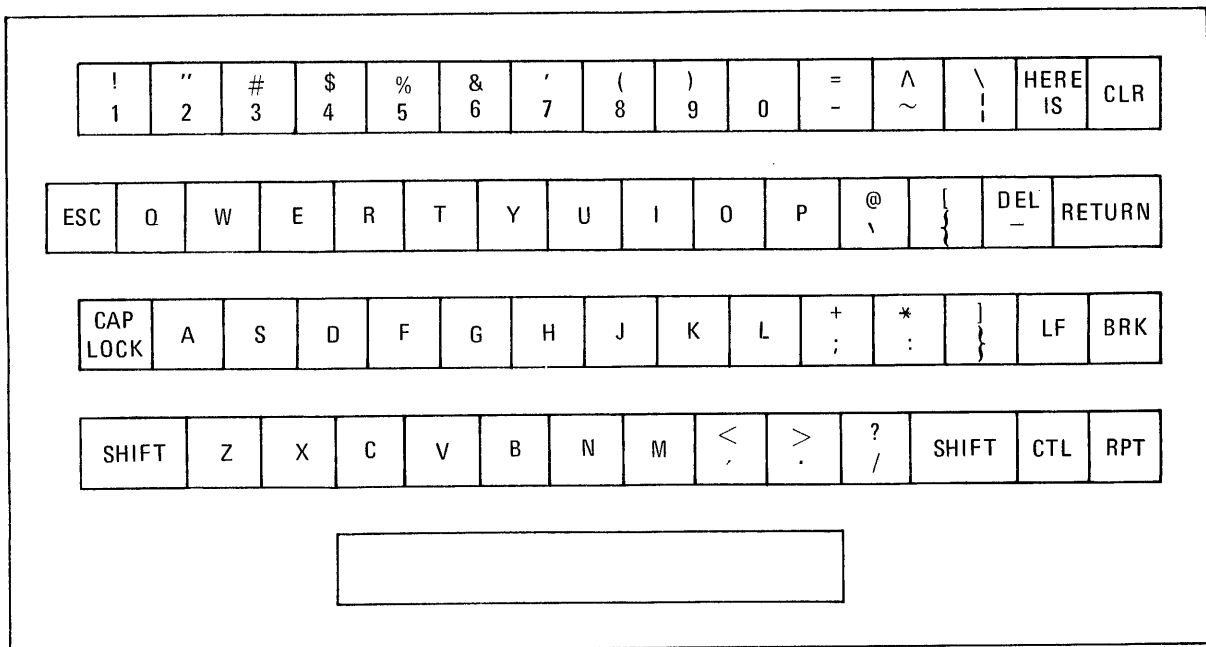
Figure 6-9. DKU9101 Keyboard

Physical Dimensions:
   17.88 in. (45.41 cm) wide; 8 in. (20.32 cm)
   deep; 3 in. (7.62 cm) high
Display
   960-character screen; 80-character line; 12
   lines; display 64 upper case ASCII charac-
   ters/95 upper and lower case ASCII characters
   with Option DKU9102, including space; 5 x 7
   character matrix; displayable screen area — 54
   square inches; character size — 0.080 x 160
   inches.
Physical Dimensions:
   18.12 in. (46.02 cm) wide; 17.50 in. (44.45
   cm) deep; 13.12 in. (33.32 cm) high; display
   and keyboard combination depth is 23.75 in.
   (60.32 cm)
Interface
   60 mA or 20 mA current loop; Bell 103A
   modem compatibility
Device Interface
   Each CRT Keyboard Console requires its own
   Device-Pac (KCM9101).

KEYBOARD TYPEWRITER CONSOLE

The TWU9101 Keyboard Typewriter Console
meets the need of users with heavy demands on
their console I/O operations (Figure 6-10). The
console prints at up to 30 characters per second
and provides 132 print positions for the 64-
character ASCII code set.

The console interfaces with the 6/30 Models by
means of a single-board Multiple Device Con-
troller (MDC9101), a Console Device-Pac
(KCM9101), and a 50-foot cable.

Features
- Print speed of up to 30 cps
- Original and up to four carbon copies
- Up to 132 print positions
- Paper-out sensor
- No fill characters required during CR/LF

Programmed Operations
- Print message on console typewriter
- Space paper
- Accept message from keyboard

Instructions
   The instructions and programming information
presented for the teleprinters (excluding paper
tape operations) is also applicable for the key-
board typewriter console.

Specifications
Print Speed:
   30 characters per second
Print Format:
   10 characters per inch, horizontal; 6 characters
   per inch, vertical
Character Set:
   64-character ASCII set
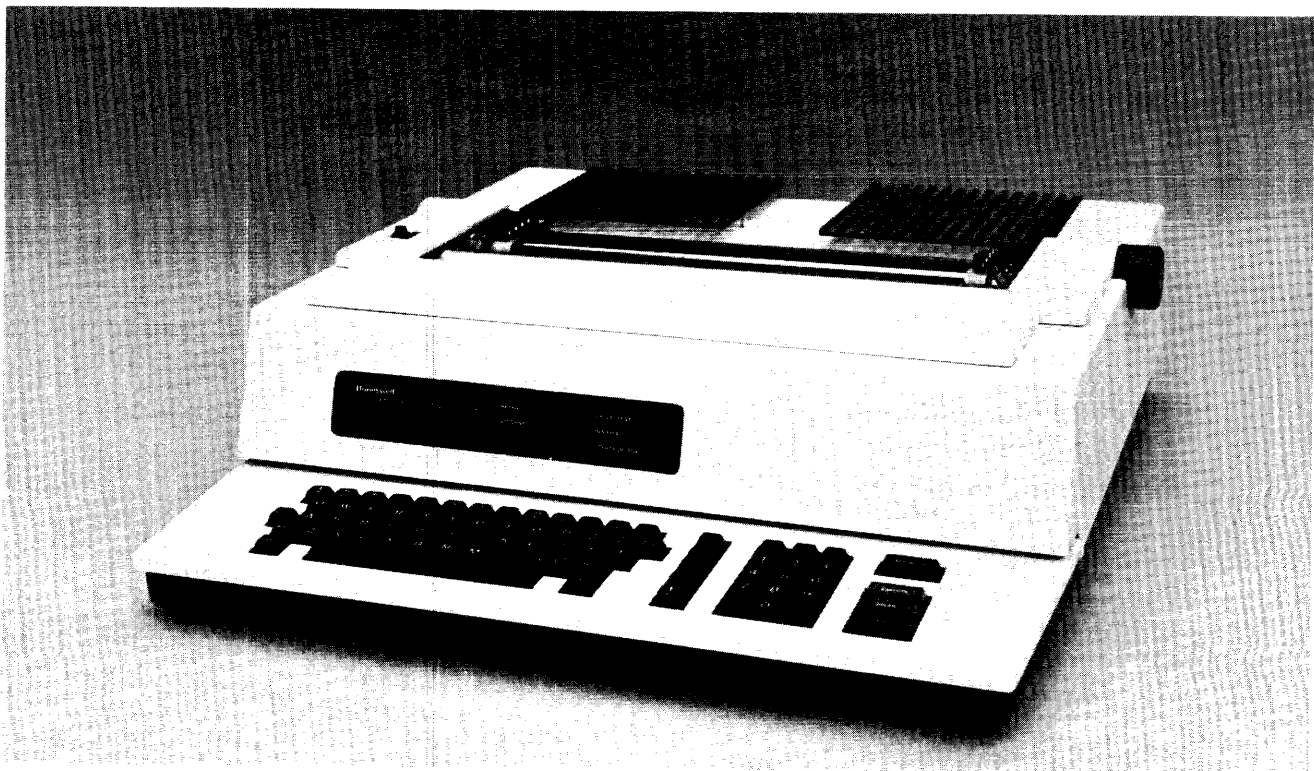
Figure 6-10. TWU9101 Keyboard Typewriter Console

Print Ribbon:
  Cartridge type, replaceable by operator
Paper Stock:
  Standard continuous fanfold paper forms with feed holes on each edge with or without margin perforations; 7.62 cm (3.0 in.) to 43.2 (17 in.) forms length; 10.16 cm (4.0 in.) to 38.1 cm (15 in.) forms width.
Device Interface:
  Each keyboard typewriter console requires its own Device-Pac (KCM9101)
Matrix Font:
  7 x 9 Dot; equivalent to 10 point type
Physical Dimensions:
  19.05 cm (7.5 in.) height; 57.15 cm (22.5 in.) width; 52.07 cm (20.5 in.) depth without keyboard, 66.04 cm (26.0 in.) depth with keyboard.

DISKETTES

The DIU9101 Single Diskette and the DIU9102 Dual Diskette provide low-cost, versatile disk storage for users of the 6/30 Models (Figure 6-11). Data is recorded on the magnetic-oxide-coated surface of an eight-inch flexible mylar disk (diskette). Each removable diskette has a data capacity of 256,256 bytes.

The diskettes are available singly (1-2 diskettes) or in a dual configuration (mix of 4 diskettes). A DIM9101 Diskette Device-Pac is required and supports up to two DIU9101 Single Diskettes or one DIU9102 Dual Diskette. The diskettes, which are offered in convenient, rack-mountable or free-standing tabletop versions, interface with the Level 6 processor by means of a single-board Multiple Device Controller (MDC9101), a Diskette Device-Pac (DIM9101), and a power supply. There is a maximum of two Device-Pacs/four diskettes per MDC.

Features
● Available in configuration of 1-4 diskettes (256KB-1,025KB)
● Use of flexible disk
  — Inexpensive media
  — Simple to load and handle
  — Easy and convenient to transport
  — Minimum storage space required
● Media compatible with IBM 3740
● Minimum operator intervention necessary
● Data integrity achieved through the use of an error detection code.
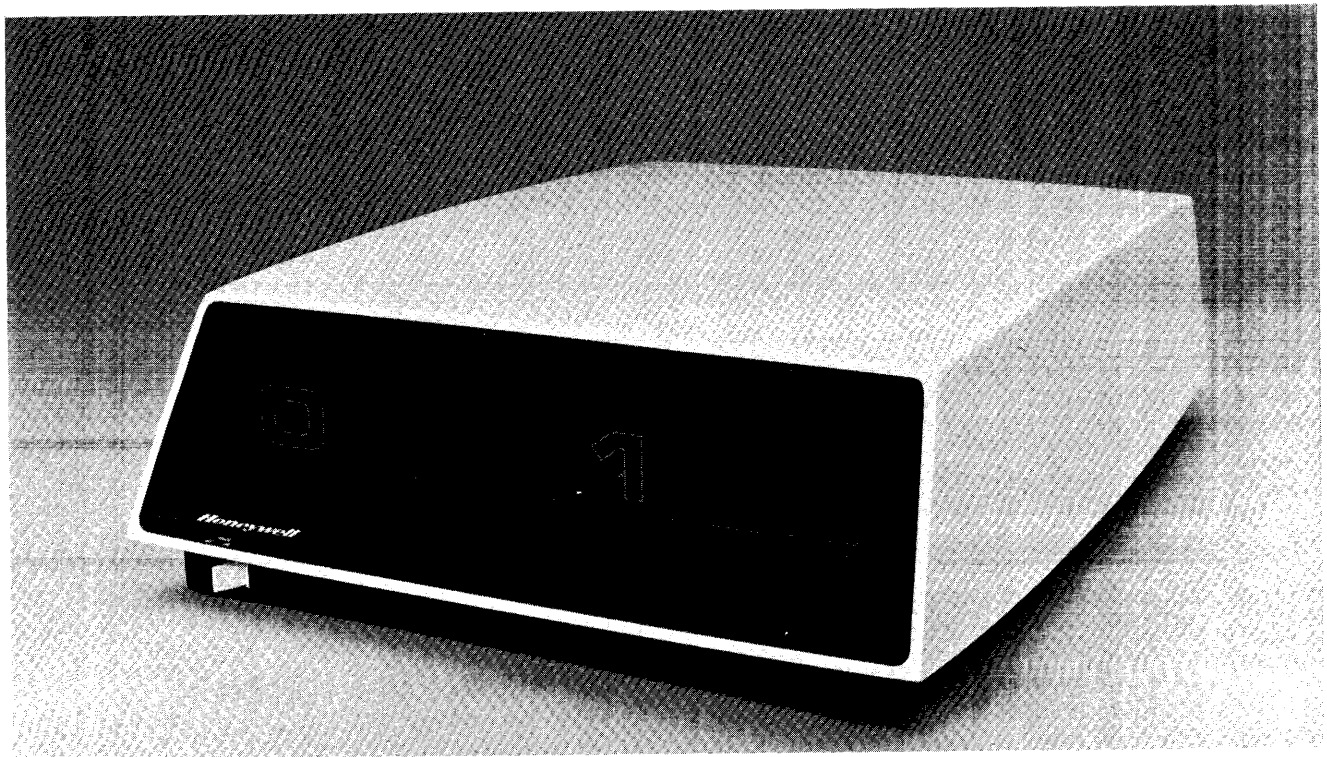
Figure 6-11. Free-Standing Tabletop Dual-Diskette

Operation

Each track on the diskette contains up to 26 equal length sectors of 128 bytes each with records starting at the beginning of a sector. There are 77 tracks yielding a total formatted capacity of 256,256 bytes. All data transfers are under DMA (Direct Memory Access) control.

While waiting for the diskette to become ready, the CP is free to perform other operations. A program interrupt signals the central processor when further device servicing is required by software.

The recording medium is composed of a single flexible disk of mylar which has a magnetic oxide coated recording surface and is packaged in a protective envelope that is never removed. The total disk package is only eight inches square.

When loading the disk, the operator lifts the diskette cover and places the envelope/disk package in position. When the cover is closed, the diskette spindle automatically engages the disk and the diskette is ready for operation.

Associated with each device (spindle) is a set of registers which are loaded by software and specify the parameters required for disk operation. In addition to range and address registers there are two configuration registers which contain record location and identification information and a task register which contains command codes. To perform a specific operation, software first loads the address, range and appropriate configuration registers (if any). The task register is loaded last and specifies the operation to be performed. The controller begins command execution when it receives the task word.

Commands addressed to a non-busy Diskette device will always be accepted but execution may be delayed if a data transfer is being performed on another diskette. All commands addressed to a busy Diskette device will be rejected (NAK response on Bus) except from an Output Control Word.

Bits 0-7 of configuration register B are treated as a sector number. This field is automatically updated by the controller during Read and Write Data Commands (see paragraphs entitled "Read Data" and "Write Data"). The sector number field of configuration register B will be incremented by one at the end of each error free data field and will point to the next sector on the track when a Read or Write operation is completed. This feature makes it unnecessary for software to update the configuration register when doing a series of sequential Read or Write Data Commands on the same track. Note that during an extended update Read or Write, records

will be processed in numerical order (not necessarily the order in which they are physically recorded). An extended operation can, therefore, be used to advantage on files that are recorded using a Sector Identifier (ID) interleaving technique as well as on files that are recorded in numerical order.

If, during a read data operation, a read error is encountered in a data field, the sector number field of configuration register B will not be incremented. The command will be terminated in this case and the sector number field will reference the sector in which the error was encountered.

Data Format

Each track on the diskette contains up to 26 equal length sectors of 128 bytes each. There are 77 tracks numbered from 0 through 76 yielding a total formatted capacity of 256,256 bytes. The data encoding scheme is double frequency recording and each field is preceded by an address mark and followed by a two byte Error Detector Code (EDC).

The Sector ID fields are software programmable and do not have to be numerically sequential. Note that the third byte of the Sector ID fields will be treated by the diskette subsystem as a sector number.

When a track is formatted, up to 26 sectors are written beginning at the index. The sector headers are specified by software and are extracted from memory during the format operation. This allows software to specify any sequence of sector IDs it may require to implement various interleaving schemes. Data will be read from memory to format up to 26 sector IDs (see paragraph entitled "Format Write." Data fields will be zero filled during formatting.

Records may be deleted from any point on a track with the "Write Deleted Data" command. This operation causes the data field of the addressed record to be updated in the normal way except that a special "deleted data field" address mark will be used to identify the field as having been deleted. This record will be automatically passed over in subsequent Read Data commands.

Track Format

The diskette track format is illustrated in Figure 6-12.

Pre-Index Address Mark Gap (GAP 1)

This field begins at the leading edge of Index Pulse and is comprised of 40 hexadecimal 00 of FF bytes. This field may, in some cases, be 47 bytes long.
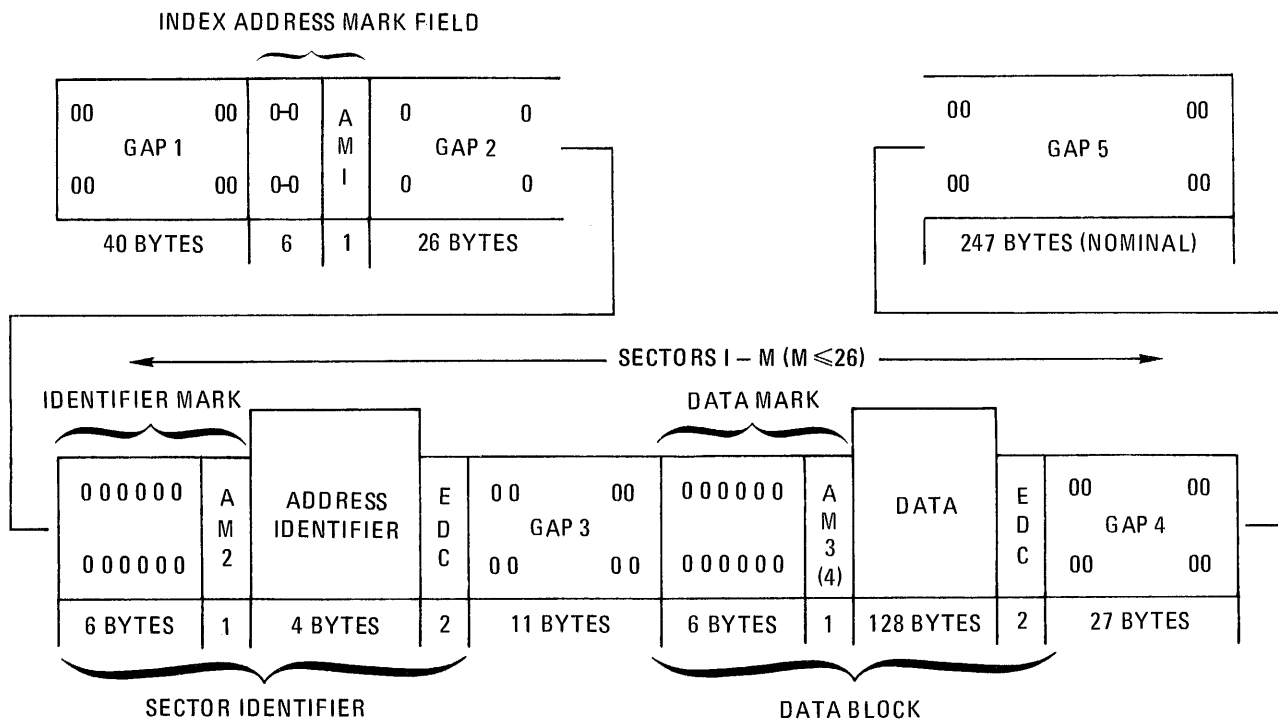
Figure 6-12. Diskette Track Format

Index Address Mark Field

This is an optional field which, when included, is comprised of 6 hexadecimal 00 bytes and one Address Mark byte (AM1). The Index Address Mark byte is illustrated in Figure 6-12. If this field is not included, the corresponding area on the track becomes part of the Pre Index Address Mark Gap. In this case the Pre Index Address Mark Gap is 47 bytes long.

Post Index Address Mark Gap (GAP 2)

This field begins with the first byte after the Index Address Mark field (or is an extension of the Pre Index Address Mark Gap if the Index Address Mark is omitted) and is comprised of 26 hexadecimal 00 or FF bytes.

Sector Identifier

The Sector Identifier Field is illustrated in Figure 6-13.
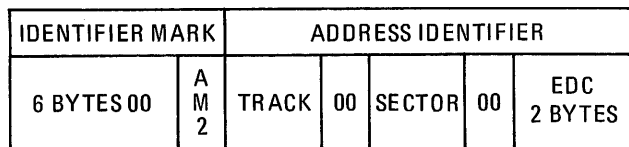
Figure 6-13. Sector Identifier

Identifier Mark

This field is comprised of 6 hexadecimal 00 bytes and a Sector Identifier Address Mark (AM2 — see Figure 6-13. Any noise areas in a preceding gap caused by write current turn-on or turn-off transients must not extend into this field.

Address Identifier

The first byte of the Address Identifier field (Track Number) is a binary number which represents the logical track number starting with hexadecimal 00 for the outermost track and increasing toward the center of the diskette. For some media, defective tracks may be skipped and the track address numbering continued sequentially with the next good track.

The second and fourth bytes of the Address Identifier field are reserved for future use (must be set to hexadecimal 00 by software).

The Sector Number byte (third byte of the Address Identifier field) is the binary representation of the sector number. This can be of any value from zero to 255 (hexadecimal FF). The order in which sectors are numbered or recorded on the diskette is not restricted by the hardware.

The last two bytes of the Address Identifier field are EDC bytes. These bytes are hardware generated by shifting serially the bits of the associated field through a 16 bit shift register (initialized to all one bits).

The last two bytes of the Address Identifier field are generated using the bytes of the Sector Identifier starting with the Sector Identifier Address Mark (AM2) and ending with the fourth byte of the Address Identifier field.

Identifier to Data Gap (GAP 3)

This field begins with the first byte after the Sector Identifier EDC bytes and is comprised of 11 hexadecimal 00 of FF bytes. These bytes may become ill-defined due to the overwriting process during data field updates.

Data Block

The Data Block field is illustrated in Figure 6-14.

DATA MARK		DATA FIELD	EDC
6 BYTES 00	A M 3	128 BYTES	2 BYTES

(OR   AM 4)
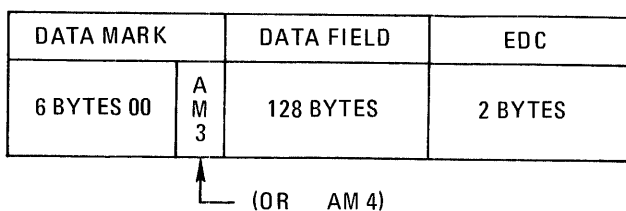
Figure 6-14. Data Block

Data Mark

This field is comprised of 6 hexadecimal 00 bytes and an Address Mark Byte. There are two types of Address Marks that can occur in front of a data field. The "Data Field Address Mark" (AM3) is for normal data fields. The "Deleted Data Field Address Mark" (AM4) indicates that the data field has been deleted. The coding of these two Address Marks is illustrated in Figure 6-12.

Data Field

Data fields are always 128 bytes long. Any write operation that does not write a complete data field will result in the rest of the field being filled with hexadecimal 00 bytes. The Format Write operation causes all the data fields on a particular track to be filled with 128 hexadecimal 00 bytes.

The last two bytes of the Data Block are EDC bytes. These bytes are generated using the bytes of the Data Block starting with the Address Mark byte (AM3 or AM4) and ending with the 128th byte of the Data Field.

Data Block Gap (GAP 4)

This field is comprised of 27 hexadecimal 00 or FF bytes. The Data Block Gap is recorded after each Data Block and precedes the following Sector Identifier. After the last Data Block on the Track this field precedes the Track Gap.

Track Gap (GAP 5)

This field follows the last Data Block Gap on the track and will contain hexadecimal 00 or FF bytes until the Index is detected. The length of this gap is dependent on the speed of the particular drive on which the medium is mounted when it is formatted or updated (nominally 247 bytes).

Defective Track Handling

Although new diskette media are shipped free of defective areas, spots on which records cannot be successfully written can develop. If disk errors begin to occur, a decision will have to be made regarding replacement of individual diskettes. If diskettes are physically damaged (torn, folded, creased, etc.) or if the recording surface becomes contaminated with a foreign material the diskette must be replaced. If, however, a bad spot develops due to excessive wear on a particular track, then it may be desirable to flag the affected area as defective in order to keep the diskette in use.

On formatted diskettes, software accounts for defective sectors (or tracks) by allocating space on the diskette around the bad area. For example, if sector 2 of track 4 on a particular diskette is bad, no files will be allocated space in that sector.

Instructions

Table 6-12 lists the I/O commands to which the MDC/Diskette Device-Pac/diskettes respond. A detailed description of each command follows this table.

TABLE 6-12. DISKETTE COMMANDS

Type	Function Code	Command
Output	09[a]	Output Address
	0D	Output Range
	11	Output Configuration Word A
	13	Output Configuration Word B
	03	Output Interrupt Control
	07	Output Task Word
	01	Output Control Word
Input	0C	Input Range
	10	Input Configuration Word A
	12	Input Configuration Word B
	02	Input Interrupt Control
	26	Input Device ID
	06	Input Task Word
	18	Input Status Word

[a]Function Code 09 as executed by the CP will result in execution of functions 09 and 0D.

Output Commands

Command:
  Output Address

Function Code:
  09

Format:

```
          Address Bus
0          7 8        17 18      23
| Module Number | Channel Number | 0 0 1 0 0 1 |

          Data Bus
0                         15
|        Byte Address        |
```

Function:
  This instruction loads a 24 bit address into the address register associated with referenced channel (device). The address refers to the starting (byte) location in main memory where the controller will commence input or output data transfers. Bits 0-7 of the Address Bus (Module Number) are the most significant bits of the address. The Data Bus contains the 16 least significant bits. Data transfers to or from memory will normally be on a word basis but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary. If an odd address is delivered by this instruction for a data transfer operation in Freeze Address Mode (see "Output Control Word") all memory read or write cycles will be in byte mode. If an even address is used in Freeze Address Mode, all memory read or write cycles will be in Word mode.

Command:
  Output Range
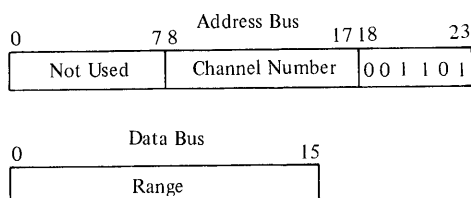
Function Code:
  0D

Format:

```
          Address Bus
0          7 8       17 18      23
| Not Used | Channel Number | 0 0 1 1 0 1 |

          Data Bus
0                      15
|         Range         |
```

Function:
  This instruction loads the Range register associated with the referenced channel. The (16 bit) quantity loaded (data bus) is the number of bytes to be transferred during the data transfer that is being set up. The number is a positive binary quantity (bit 0 must be zero) and is decremented by the controller after each memory transfer. A range of zero will result in a premature End-of-Operation termination for any read or write command that may be subsequently issued (see Output Task Word).

Command:
  Output Configuration Word A
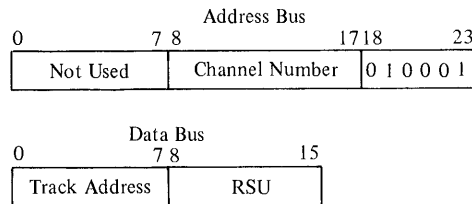
Function Code:
  11

Format:

```
          Address Bus
0          7 8       17 18      23
| Not Used | Channel Number | 0 1 0 0 0 1 |

          Data Bus
0          7 8       15
| Track Address | RSU |
```

Function:
  This instruction loads Configuration Word A for the device corresponding to the referenced channel. The Track Address (bits 0-7) is used as the seek argument during seek operations. The complete word is used as the two high order bytes of a Sector ID field to be searched for during an update Read or Write operation. Bits 8-15 are reserved for software use (RSU). IBM formatted diskettes will have zeroes in these bits.

Command:
  Output Configuration Word B
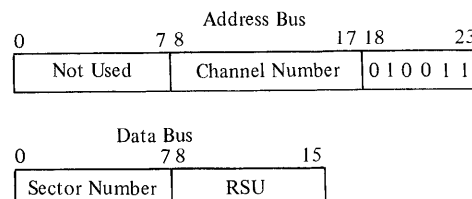
Function Code:
  13

Format:

```
          Address Bus
0          7 8       17 18      23
| Not Used | Channel Number | 0 1 0 0 1 1 |

          Data Bus
0          7 8       15
| Sector Number | RSU |
```

Function:

This instruction loads Configuration Word B for the device corresponding to the referenced channel. This word is used as the low order two bytes of a Sector ID field to be searched for during an update Read or Write operation. The subsystem will treat bits 0 through 7 of Configuration Word B as a sector number. This number will be incremented after operating on a data field during an update Read or Write operation. Bits 8-15 are reserved for software use (RSU). IBM formatted diskettes will have zeroes in these bits.

Command:
Output Interrupt Control

Function Code:
03

Format:

```
               Address Bus
0            7 8            17 18    23
 ┌──────────┬─────────────┬────────┐
 │ Not Used │Channel Number│0 0 0 0 1 1│
 │          │(of Diskette) │        │
 └──────────┴─────────────┴────────┘

             Data Bus
0              9 10       15
 ┌──────────────┬─────────┐
 │Channel Number│Interrupt│
 │(of CP )      │Level    │
 └──────────────┴─────────┘
```

Function:

This instruction loads, for the referenced device, the interrupt level and the channel number of the CP to which subsequent interrupts should be sent. The level number is a 6 bit quantity and is positioned on the data bus as illustrated above. Bits 0-9 of the data bus contain the channel number of the CP loading the Interrupt Level. If an Interrupt Level of zero is loaded, the subsystem will not generate or save interrupts for any events that occur while the Interrupt Level is zero. The Interrupt Level is set to zero whenever the subsystem is initialized.

Command:
Output Task Word

Function Code:
07

Format:

```
               Address Bus
0            7 8            17 18    23
 ┌──────────┬─────────────┬────────┐
 │ Not Used │Channel Number│0 0 0 1 1 1│
 └──────────┴─────────────┴────────┘

           Data Bus
0            7 8          15
 ┌──────────────┬─────────┐
 │              │Not Used │
 └──────────────┴─────────┘
```

```
0 X X X X X X 0 ───── Recalibrate
0 X X X X X X 1 ───── Seek
1 0 X X X B X 0 ───── Format Read/Write
1 0 X X X 0 0 1 ───── Data Field Read/Write
1 0 X X X 1 0 1 ───── Deleted Data Field Read/Write
1 0 X X X A 1 1 ───── Diagnostic Read/Write
1 1 X X X X X X ───── Wraparound Read/Write

        Applicable for Read only
          1 - Read ID Fields only
          0 - Read ID and Data Fields

        Applicable for Write only
          1 - Use Deleted Data Field Address Marks
          0 - Use Normal Data Field Address Marks

        X = Assumed zero's (not checked)
```

Function:

This instruction outputs a Task Word to the referenced channel. The coding of bits 0-7, illustrated above, represent the operations that are to be performed. When this instruction is accepted, the channel enters the Busy state and execution of the indicated task is immediately begun. All address, range and configuration information must be loaded prior to execution of this instruction. The direction of data transfer is indicated on the low order bit of the channel number used in the most recent output address instruction.

The individual bits will cause the following to occur:

- Recalibrate: The Recalibrate command causes the channel to move the device's positioner to track zero and reset the "Device Fault" line on the device interface (via the "Fault Reset" line). This instruction is intended as an Initialization command to guarantee that the positioner location information in the controller is correct and that the device faults are cleared.

- Seek: The Seek command in the Task Word causes the channel to move the device's positioner to the track indicated in Configuration Word A. If the device indicates that it is on track zero when not expected, a cylinder number greater than 76 is specified in Configuration Word A or the device cannot be positioned at track zero during a Recalibrate command (as indicated by the "Track Zero" line) then the seek Error Bit will be set in the Status Word.

- Format Read: The Format Read command causes the channel to read all Identifier (ID) fields (for Task Word bit 5=1) or all Identifier and Data Fields (for Task Word bit 5=0 — including deleted data fields) on a track beginning with the first sector after index and in the order in which they are recorded. Data will be transferred to memory beginning at the memory location specified in the subsystem's memory address register. This address will be the address loaded by the most recent Output Address instruction if no data transfer has occurred since that instruction was executed. If one or more data transfer operations have been executed since the last Output Address instruction, then the starting memory address used for this operation will be the byte address immediately following the end of the most recent data transfer executed for this device (either read or write).

Data will be transferred until a read error occurs, the range is satisfied, or the entire track is read (index is detected).

Normal range for this command (to read one complete track) is

$$R = (4 + 128) \times 26 = 3432 \text{ bytes}$$

where;

- 4 = ID
- 128 = Data
- 26 = Sectors

If this command is terminated due to end of track before the range is satisfied, the residual range will be available via the Input Range command.

A read error in any field transferred to memory will cause the operation to be terminated with the Read Error bit set in the Status Word. The Sector ID field in Configuration Word B will point to the record in error. The field in error can be determined through examination of the residual range (if a read error is detected in an ID field the range will have been decremented for the ID field only).

If the required transfer rate is not maintained on the Bus (15.6 KW/S), the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

If the range register is zero when this command is received the Task will be immediately terminated (End-of-Operation). No data will be read or transferred.

- Format Write: The Format Write command causes the channel to format the track which is positioned under the Read/Write head when this command is received. Up to twenty-six equal length sectors will be written starting at index. The Secor ID fields will be read from memory beginning with the memory location specified in the subsystem's memory address register.

Data fields will be written with normal data field Address Marks and will be zero filled.

The range to format one complete track is:

$$R = 4 \times 26 = 104 \text{ bytes}$$

If a range less than 104 is sent for a format write, the track will be zero-filled (may result in fewer than 26 sectors). If the range expires after the first word of a sector ID field, then the second word of that ID is unspecified. If a range greater than 104 is specified, a partial sector might be recorded (a sector can be started in the Track Gap but will not be completed if the Index Pulse is detected before the end of the Data Field). If the range register is zero when this command is received, the Task will be immediately terminated (End-of-Operation). No data will be written.

If the Sector ID data cannot be read from memory at a sufficient rate, then the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

- Read Data: The Read Data command causes the channel to locate the sector defined by the Sector ID image loaded in Configuration Words A and B and to transfer the data field of (at least) that sector to main memory. Data will be transferred to memory beginning with the memory location specified in the subsystem's memory address register and

will continue until the range is satisfied. When the transfer of the first specified sector data field is completed (without error), the Sector Number field of Configuration Word B will be incremented (module 256). If the initial range is greater than 128 then the sector represented by the updated contents of Configuration Words A and B (A is unchanged) will be located and data transfer will continue until either the range is satisfied, a read error occurs or the record specified by Configuration Words A and B cannot be located on the track (as indicated by the detection of two index marks without a successful compare). If the specified record cannot be located, then an unsuccessful search will be posted in the Status Word (bit 7).

If a deleted Data Address Mark is encountered during a Read Data operation, that field will be spaced over and the Read continued on the numerically next sector (Deleted Field bit set in the Status Word — bit 3).

If a read error is encountered in a data field the operation will be set (bit 4). The Sector Number field of Configuration Word B will contain the address of the record in error. If a read error is encountered in an ID field, a miscompare result will be assumed and the search will continue. The Read Error bit will *not* be posted.

If this command is terminated before the range is satisfied the residual range will be available via the Input Range command. If the range register is zero when this command is received, the Task will be immediately terminated (End-of-Operation). No data will be read or transferred.

If the required transfer rate is not maintained on the Bus (15.6 KW/S) then the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

● Write Data: The Write Data command causes the channel to locate the sector defined by the Section ID image loaded in Configuration Words A and B and to rewrite the data field of at least that sector. The data will be read from memory beginning with the memory location specified in the subsystem's memory address register. Rewritten data fields will be preceded by normal data field address marks (see Figure 6-12).

When the transfer of the specified sector is completed, the Sector Number field of Configuration Word B will be incremented. If the range is less than 128 the data field will be zero-filled. If the range is greater than 128, the sector represented by the update contents of Configuration Words A and B (A is unchanged) will be located and the data field rewritten (preceded by a normal data field Address Mark). This operation will continue until either the range is satisfied or the record specified by Configuration Words A and B cannot be located on the track (as indicated by the detection of two index marks without a successful ID field compare). If the latter event occurs, Unsuccessful Search will be posted in the Status Word (bit 7).

If two or more records that are to be updated with a single Write Data command are physically adjacent, they will be written consecutively without loss of a revolution.

If a read error is encountered in an ID field, a miscompare result will be assumed and the search will continue. In this case the Read Error bit will *not* be posted.

If this command is terminated before the range is satisfied the residual range will be available via the Input Range command. If the range register is zero when this command is received the Task will be immediately terminated (End-of-Operation). No data will be written.

If the required transfer rate is not maintained on the Bus (15.6 KW/S) the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

● Deleted Data Read/Write: The Deleted Data encoding of the Task Word (1XXXX101) when received on a write channel (low order bit of the channel number equals 1) causes the channel to perform as if the Write Data command was specified except that each data field updated will be preceded by a Deleted Data Field Address Mark. Note that the data written in the deleted data fields will be read from memory.

If this Task Word encoding is received on a read channel the channel will perform as if the Read Data command was specified except that only data fields that are preceded by Deleted Data Field Address Marks will be read.

- Write Diagnostic: The Write Diagnostic command causes the channel to perform as if the Write Data command was specified except that invalid EDC characters will be written at the end of each data field updated (the EDC characters will always be zero).

Note that the data written in the data fields will be read from memory and the Address Marks will be as specified by bit 5 of the Task Word.

- Read Diagnostic: The Read Diagnostic command causes the channel to read everything on a track (including gaps, address marks, ID and data fields and EDC bytes) beginning with (and including) the address mark preceding the first sector Identifier on the track and ending at index pulse. Meaningful operation of this command can only be guaranteed on tracks which have not been updated since the last format operation. No EDC checks will be done. Data will be transferred until the range is satisfied or the entire track is read (index is detected). Normal range for this command (to read one complete track) is

$$R = (7 + 17 + 131 + 33) \times 26 + 247 = 5135 \text{ bytes}$$

where;

$$
\begin{aligned}
7 &= \text{Sector ID and Address Mark} \\
17 &= \text{Gap} \\
131 &= \text{Data Field plus Address Mark} \\
33 &= \text{Gap} \\
26 &= \text{Sectors} \\
247 &= \text{Track Gap}
\end{aligned}
$$

If this command is terminated due to end of track before the range is satisfied, the residual range will be available via the Input Range command.

If the required transfer rate is not maintained on the Bus (15.6 KW/S), the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

- Wraparound Read/Write: During a Wraparound Write command, the channel will read one byte from memory (at the address specified in the subsystem's memory address register, shift the byte through the diskette adapter write logic with an address mark clock bit pattern inserted, and save the resulting bit pattern (16 bits) in the adapter for use during a subsequent Wraparound Read command. The saved bit pattern will be recognizable as an address mark by the adapter read recovery and address mark detection logic. The byte supplied by software for the Wraparound Write command must have one bit in the two high order bit positions.

When a Wraparound Read command is received (immediately following a Wraparound Write) the saved bit pattern from the preceding Wraparound Write command will be shifted into the adapter read recovery and address mark detection logic as if it were a bit pattern from the medium. If no errors occur, an address mark will be detected and the byte of data (with clock bits removed) will be returned to main memory at the address specified in the subsystem's memory address register. The byte returned during this operation should be the same as the byte supplied by software in the preceding Wraparound Write command.

If, during the Wraparound Read operation, an address mark is not detected by the adapter, the operation will not be terminated. In this case, the adapter will continually shift zeros into the read recovery logic until stopped with a Stop I/O command or an Initialize (Output Control Word or Master Clear).

A range of one should always be used for these commands. If a zero range is specified the command will be immediately terminated (without being executed). Ranges greater than one for these commands result in different subsystem responses depending on the starting address and data transfer direction and should, therefore, not be used.

Command:
 Output Control Word
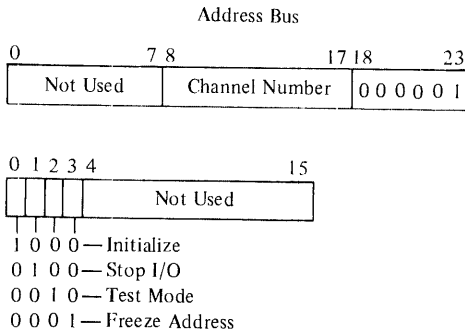
Function Code:
 01

Format:

Address Bus

```
0          7 8            17 18      23
┌──────────┬──────────────┬──────────┐
│ Not Used │Channel Number│0 0 0 0 0 1│
└──────────┴──────────────┴──────────┘
```

```
0 1 2 3 4                  15
┌─┬─┬─┬─┬──────────────────┐
│ │ │ │ │     Not Used      │
└─┴─┴─┴─┴──────────────────┘
 1 0 0 0 — Initialize
 0 1 0 0 — Stop I/O
 0 0 1 0 — Test Mode
 0 0 0 1 — Freeze Address
```

Function:

This instruction loads a Control Word into the referenced channel. This command will be unconditionally accepted by the channel regardless of its Busy status. The individual bits will cause the following specific actions to occur:

- Initialize: This command will cause the MDC to reset to the same state that it enters after power up. When an initialize command is received by the MDC all of its channels are initialized (regardless of which channel the command was received over). A Recalibrate command is issued for each diskette during execution of this instruction so that the MDC will be in a state capable of proper control of diskette devices. Any operations that are in progress in the MDC at the time of the Initialization will be abruptly terminated and all registers will be initialized. No information about the terminated operations will be retained and no interrupts for the operations will be generated. The interrupt level for all channels will be set to zero (interrupts blocked).
- Stop I/O: This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress it will not be completed nor will any error checking be done. If a diskette positioner is in motion when this command is received, positioner orientation information will be lost. An interrupt will be generated for the operation terminated by this command as if the operation had come to a normal ending point. Status, Address and Range information, present in the MDC when this command is received, will be retained.
- Test Mode: Refer to paragraph entitled "Test Mode."

- Freeze Address: When this bit is set, all DMA data transfers on this channel will come from or go to the same memory location. The address in the channel's memory address register will not be incremented. Note that if an odd address is specified in freeze address mode all memory read or write cycles will be in byte mode. This effectively doubles the transfer rate of a diskette to 31.2 KB/S. If an even address is specified, all memory read or write cycles will be in word mode.

Once set, this bit will remain set until another Output Control Word is received or the MDC is Initialized (Master Clear or Initialize command on any MDC channel).

Input Commands

Command:
Input Range

Function Code:
0C

Format:

Address Bus

```
         0          7 8              17 18      23
Instruction ┌──────────┬──────────────┬──────────┐
Cycle       │ Not Used │Channel Number│0 0 1 1 0 0│
            │          │  (Diskette)  │          │
            └──────────┴──────────────┴──────────┘
            Data Bus
            0                9 10      15
            ┌────────────────┬─────────┐
            │ Channel Number │         │
            │     (CP)       │         │
            └────────────────┴─────────┘
```

```
         0          7 8              17 18      23
Response   ┌──────────┬──────────────┬──────────┐
Cycle      │ Not Used │Channel Number│          │
           │          │    (CP)      │          │
           └──────────┴──────────────┴──────────┘
           Data Bus
           0                             15
           ┌──────────────────────────────┐
           │        Range Register          │
           └──────────────────────────────┘
```
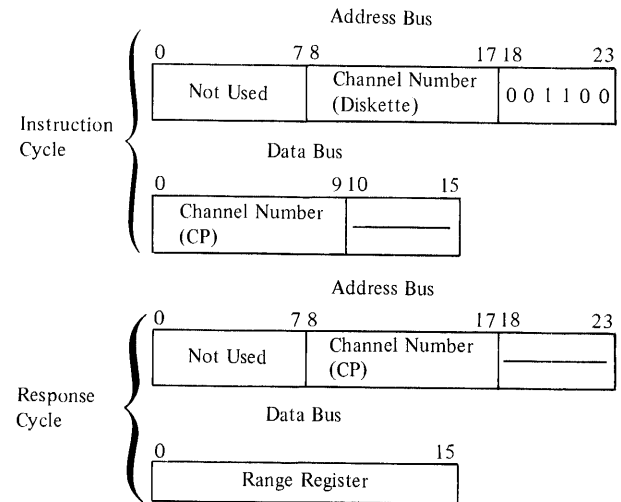
Function:

This instruction causes the contents of the referenced channel's Range register to be transferred to the requesting channel.

During the Response cycle (Second Half Read) the MDC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle.

Command:
  Input Configuration A

Function Code:
  10

Format:

Address Bus

```
0              7 8              17 18        23
┌──────────────┬──────────────┬────────────┐
│   Not Used   │Channel Number│ 0 1 0 0 0 0│  "A"
│              │  (Diskette)  │ 0 1 0 0 1 0│  "B"
└──────────────┴──────────────┴────────────┘
```

Instruction Cycle

Data Bus

```
0                    9 10        15
┌────────────────────┬────────────┐
│  Channel Number    │  _____  │
│  (CP)              │            │
└────────────────────┴────────────┘
```

Address Bus

```
0              7 8              17 18        23
┌──────────────┬──────────────┬────────────┐
│   Not Used   │Channel Number│  _____  │
│              │    (CP)      │            │
└──────────────┴──────────────┴────────────┘
```

Response Cycle

Data Bus

```
0                                        15
┌──────────────────────────────────────────┐
│      Configuration Word A (B)            │
└──────────────────────────────────────────┘
```

Function:
  This instruction causes the channel's Configuration Word A (B) to be transferred to the requesting channel.
  During the Response cycle (Second Half Read) the MDC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle.

Command:
  Input Configuration Word B

Function Code:
  12

Format:
  See "Input Configuration Word A"

Function:
  See "Input Configuration Word A"

Command:
  Input Interrupt Control

Function Code:
  02

Format:

Address Bus

```
0              7 8              17 18        23
┌──────────────┬──────────────┬────────────┐
│   Not Used   │Channel Number│ 0 0 0 0 1 0│
│              │  (Diskette)  │            │
└──────────────┴──────────────┴────────────┘
```

Instruction Cycle

Data Bus

```
0                    9 10        15
┌────────────────────┬────────────┐
│  Channel Number    │  _____  │
│  (CP)              │            │
└────────────────────┴────────────┘
```

Address Bus

```
0              7 8              17 18        23
┌──────────────┬──────────────┬────────────┐
│   Not Used   │Channel Number│  _____  │
│              │    (CP)      │            │
└──────────────┴──────────────┴────────────┘
```

Response Cycle

Data Bus

```
0                      9 10        15
┌──────────────────────┬────────────┐
│ Channel Number (CP   │            │
│ which last loaded    │   Level    │
│ this register)       │            │
└──────────────────────┴────────────┘
```

Function:
  This instruction causes the channel's Interrupt Level to be transferred to the requesting channel. The level value will be placed on Data Bus bits 10 through 15 (see above) with bit 15 as the least significant bit. This quantity is the value previously received in an Output Interrupt Control Instruction, or, a default value of 00. The default value is the Interrupt Level assumed by the channel when initialized. Note that the channel number returned in bits 0-9 of the Data Bus might be different than the channel number of the CP executing this instruction if more than one CP is attached to the Bus.
  During the Response cycle (Second Half Read) the MDC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle.

Command:
  Input Device ID

Function Code:
  26

Format:

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Diskette)	1 0 0 1 1 0	

Data Bus

0	9 10	15
Channel Number (CP)		

Instruction Cycle

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)		

Data Bus

0	15
Identification Code	

Response Cycle

Function:

This instruction will cause the referenced channel to transfer its identification code to the requesting channel. The code for this type of Diskette is 2010 (Hex).

During the Response cycle (Second Half Read) the MDC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle.

Command:
Input Task Word

Function Code:
06

Format:

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Diskette)	0 0 0 1 1 0	

Data Bus

0	9 10	15
Channel Number (CP)		

Instruction Cycle

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)		

Data Bus

0	15
Task Word	

Response Cycle

Function:
This instruction causes the Task Word of the referenced channel to be transferred to the requesting channel. The Task Word transferred will contain the code for the last operation executed by the channel (unless an Initialize has occurred).

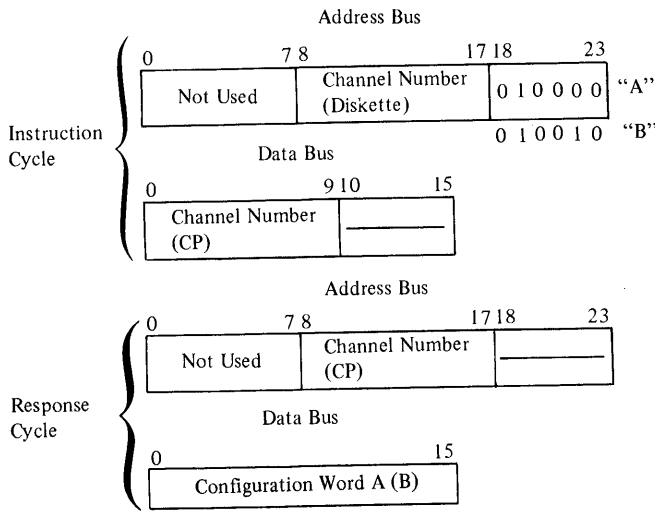During the Response cycle (Second Half Read) the MDC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle.

Command:
Input Status Word

Function Code:
18

Format:
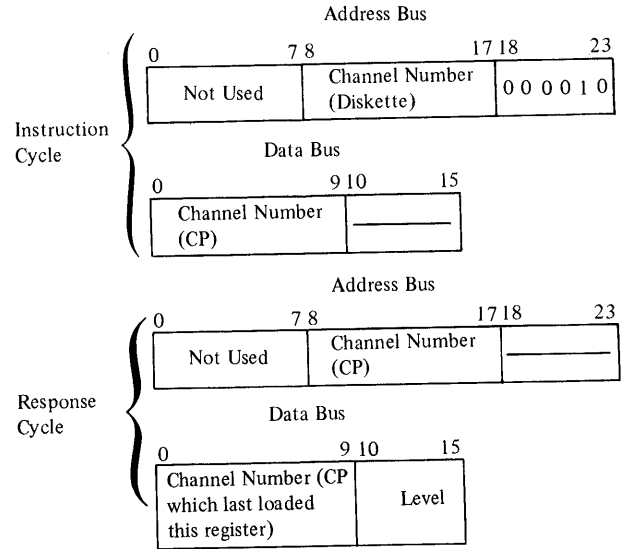
Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Diskette)	0 1 1 0 0 0	

Data Bus

0	9 10	15
Channel Number (CP)		

Instruction Cycle

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)		

Data Bus

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

0   Device Ready
1   Attention
2   Overrun/Underrun
3   Deleted Field
4   Read Error
5   Device Fault
6   Missed Data Sync.
7   Unsuccessful Search
8   Not Used
9   Not Used
10 Seek Error
11 Not Used
12 Corrected Memory Error
13 Non-Existent Resource
14 Bus Parity Error
15 Uncorrected Memory Error

Response Cycle

Function:
This instruction causes the referenced channel's Status Word 1 to be transferred to the requesting channel.

During the Response cycle (Second Half Read) the MDC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle. See also Table 6-13.
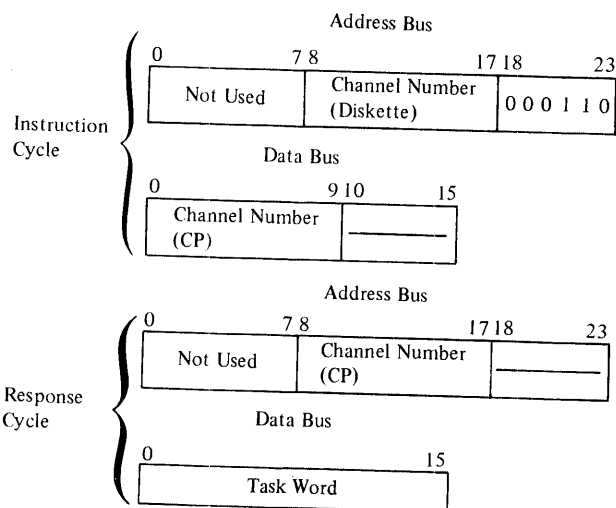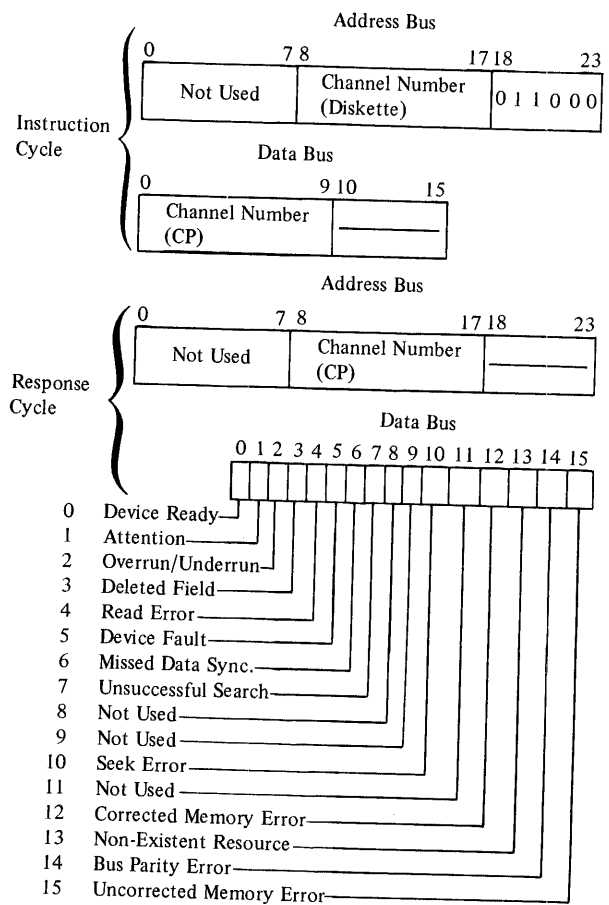
TABLE 6-13. STATUS BIT DEFINITIONS – DISKETTE

Status Condition	Bit	Definition	Reset By
Device Ready	0	This bit indicates that the device is on line with the medium loaded and that no further manual intervention is required to place it under program control. Note that a change of state of this bit will cause the Attention bit (bit 1) to be set resulting in an interrupt (if the interrupt level is non-zero).	A change in condition.
Attention	1	This indicator will be set whenever the Device Ready bit (bit 0 of the status word) changes state. Any change of operational status of the device (e.g., load/unload of media) will be indicated to software in this way. Whenever the Attention bit is set an interrupt is attempted (if the interrupt level is non-zero). If a previously initiated operation is in progress when a device state change is sensed the resultant interrupt (with the Attention bit set) will serve as notification of both the end of the operation and the device state change.	Output Control Word,[1] Input Status Word, Output Task Word, or Master Clear on the bus
Overrun/Underrun	2	This bit is set during a Read or Write operation when the data transfer to/from main memory cannot be maintained at a high enough rate (15.6 KW/s during field transfers in word mode). Either data was lost on input because of failure to keep up with device demands or data was unavailable on output when required by the device.	Output Control Word,[1] Output Task Word, or Master Clear on the bus
Deleted Field	3	This bit will be set if a Deleted Data Field Address Mark is encountered during a Format Read command or if a data field which would normally by read during a Read Data command is skipped because of a Deleted Data Field Address Mark. This bit will also be set if the Deleted Data Field encoding of the Task Word (1XXXX101) is received on a Read channel and a normal data field is skipped during the resulting read operation. Posting of this indication does not cause the operation in progress to be terminated.	Same as preceding bit.
Read Error	4	This bit is set during any Read operation if the EDC Word at the end of a field disagrees with the EDC Word calculated while reading the field.	Same as preceding bit.
Device Fault	5	This bit will be set whenever a Fault indication is received from the device.	Recalibrate, Output Control Word,[1] or a Master Clear on the bus

[1] Initialize encoding only.

TABLE 6-13 (cont). STATUS BIT DEFINITIONS — DISKETTE

Status Condition	Bit	Definition	Reset By
Missed Data Sync	6	This bit will be set if, after a Sector ID has been detected during a Read operation, the corresponding data field is not detected or if during a Format Read two consecutive Data field (or two consecutive ID field) address marks are detected (indicating that a field was missed).	Output Control Word,[1] Output Task Word, or a Master Clear on the bus.
Unsuccessful Search	7	This bit is set during a non-format Read or Write operation for which the Sector ID specified in Configuration Words A and B cannot be located on the Track.	Same as preceding bit.
Seek Error	10	This bit is set during a Seek operation if the device indicates that it is on track zero when not expected, if a cylinder number greater than 76 is specified in Configuration Word A or if the device cannot be positioned at track zero (as indicated by the 'Track Zero' line) during a Recalibrate command.	Output Control Word,[1] Recalibrate, or Master Clear on the bus.
Corrected Memory Error	12	This bit indicates that during execution of the previous operation Main Memory detected and corrected a memory read error. The data that was delivered to the MDC was assumed to be correct.	Output Control Word,[1] Output Task Word or Master Clear on the bus.
Non-Existent Resource	13	This bit is set whenever the MDC attempts a Write or Read request Bus cycle and receives a NAK response.	Same as preceding bit.
Bus Parity Error	14	This bit is set whenever the MDC detects a parity error on either byte of the Data Bus during any Output bus cycle (i.e., odd function code), during a second half memory read cycle or when a parity error is detected in bits 0—7 of the Address Bus during an Output Address command.	Same as preceding bit.
Uncorrected Memory Error	15	This bit indicates that during execution of the previous operation Main Memory detected a read error which the EDAC algorithm could not correct. The data that was delivered to the MDC was incorrect. Occurrence of this condition will not cause termination of the operation in progress (may result in bad data written on the medium).	Same as preceding bit.

[1] Initialize encoding only.

Specifications

- Seek Time: 20 milliseconds minimum (track to track includes head settling time); 260 ms average; 770 ms maximum.
- Latency Time: 83.33 ms average rotational latency
- Transfer Rate: 249,984 bits/second (Device-Pac to diskette; 31,248 bytes/second or 16,124 words/second

- Data Capacity: 256,256 bytes/disk (formatted-77 tracks); 3,328 data bytes/track (formatted)
- Diskette Speed: 360 rpm
- Tracks Per Disk Surface: 77
- Recording Density: 3200 bpi
- Device Interface: A Diskette Device-Pac (DIM9101) is required for each DIU9102 or

for up to two DIU9101s.
- Medium: Honeywell Type M4101 (or equivalent)
- Physical Dimensions: 10.47 in. (26.59 cm) high; 17.5 in. (44.45 cm) wide; 22 in. (55.88 cm) deep.

CARTRIDGE DISK UNITS

The Cartridge Disk Units provide low-cost data storage for 6/30 Model users with medium-sized file requirements (Figure 6-15). Storage capacities of 2.5 to 10.0 (12 sectors/track) or 2.8 to 11.2 (24 sectors/track) million bytes are available for a single device, with up to four devices capable of being connected to one controller.

The units are rack-mountable and they pull out from the front to provide easy access for top-loading the removable cartridge. Both a removable and a fixed disk can be mounted on the same spindle, thus providing a file copying capability with a single device. File protect switches control each disk separately.

The Cartridge Disk Units are available in models with either a removable cartridge only, or with both a removable and a fixed disk. These are further divided into low density units with data recorded at 100 tracks per inch (tpi) and high density units recorded at 200 tpi. There are thus four different units available with data capacities as follows:

- CDU9101 Cartridge Disk Drive, low density, removable disk only — 2.5/2.8 million bytes
- CDU9102 Cartridge Disk Drive, low density, fixed and removable disks — 5.0/5.6 million bytes
- CDU9103 Cartridge Disk Drive, high density, removable disk only — 5.0/5.6 million bytes
- CDU9104 Cartridge Disk Drive, high density, fixed and removable disks — 10.0/11.2 million bytes.

The Cartridge Disk Units interface with the Level 6 processor by means of a Mass Storage Controller (MSC9101) and a Cartridge Disk Device-Pac (CDM9101). The MSC9101 can connect and control up to four CDU9101/9102 low density units or up to four CDU9103/9104 high density units.
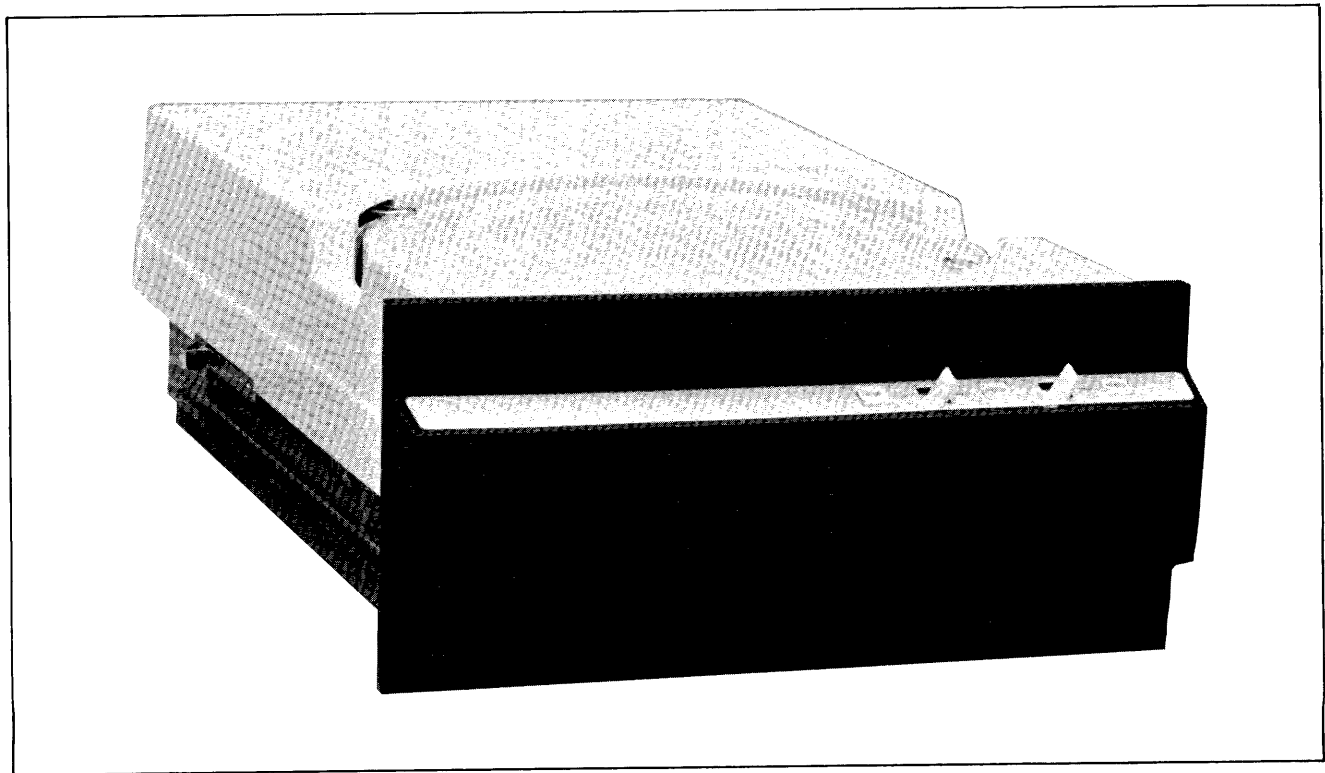
Figure 6-15. CDU9101/9102/9103/9104 Cartridge
Disk Units

Features

- Combines transportability of magnetic tape with random access features of disk
- Ideal for applications requiring fast access to a medium-sized data base; average random access to 10 million bytes is less than 50 milliseconds
- Maximum total data storage capacity of 40.1/45.1 million bytes; Direct Memory Access transfers data at 156K words/second
- 200 tpi recording allows 408 cylinders per spindle, each with a capacity of 12 or 24K bytes accessible with no head movement
- Up to four disk units per control; choice of all high or all low density disk drives
- Record length can be varied to suit customer application; all records include check words for data integrity
- Each track can have a maximum of 12 or 24 individually addressable records; software interlace of record addresses minimizes rotational latency time
- Single removable cartridge disk or removable and fixed cartridge disk units; disk-to-disk copying capability on the same unit.

Operation

Depending upon the format selected, each track consists of 12/24 fixed length sectors that are clocked by fixed slots inscribed into the circumference of a disk. Records start at the beginning of a sector, with a maximum of 12/24 records of up to 576/256 bytes each per track. Larger records can be written linking two or more sectors. The maximum record length is 6912 (12x576)/6144 (24x256) bytes, linking all 12/24 sectors on one track. See Figure 6-16).

To seek a particular cylinder and disk, a word containing the record location must be output to the controller. A second setup word is also output that contains the track and header (sector number) of the record to be written or read.

Each record consists of two parts:

Header — One 32-bit record identifier
Data — From 256 or 576 byte sectors

Each part is followed by a check word that is automatically validated on read operations.

There are four modes of reading or writing:

TOP VIEW

TRACKS DIVIDED INTO 12/24
SECTORS, EACH SECTOR
INDIVIDUALLY ADDRESSABLE

TRACK 407

TRACK 0

204ª TRACKS (LOW-DENSITY UNIT,
100 TRACKS PER INCH) OR
408 TRACKS (HIGH-DENSITY UNIT,
200 TRACKS PER INCH)
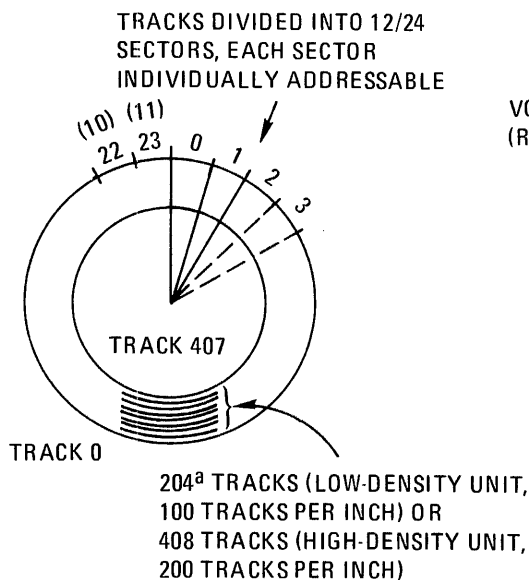
ªNOTE: EVEN TRACK ADDRESSES ONLY
(0, 2, 4 . . . 406) ON LOW DENSITY UNIT.

SIDE VIEW

HEAD NUMBER

VOLUME 0
(REMOVABLE)

VOLUME 1
(FIXED)

HEADS POSITIONED
IN PARALLEL TO
SAME TRACK ON
ALL FOUR SURFACES
(ONE CYLINDER)

MOVEMENT

SPINDLE
2400 RPM
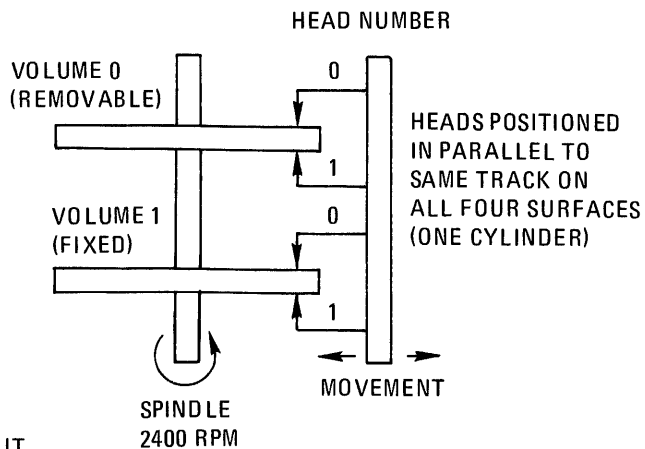
Figure 6-16. Physical Organization of Cartridge Disk

- write format
- write record
- read record
- read track (headers or headers and data)

All reads and writes are under control of Direct Memory Access (DMA), with the address and range registers in the controller describing the area in memory that is being written from or read into.

The first operation that must be performed is a write format operation which writes 12 or 24 headers, one per sector, on a track, and zero fills the data fields. A write record then writes a single record which may consist of multiple sectors after matching on the proper header. Writing is terminated either by DMA end-or-range or by reading the end-of-track. A read operation again matches on a header and reads data until an end-of-range is reached. A read-track operation reads the header words and data starting with Sector 0 in succession until an end-of-track or end-of-range is reached.

Data Format

Each track on the disk contains 12 or 24 equal length sectors of 256 or 576 bytes, respectively. There are 204 or 408 cylinders per surface and 2 or 4 tracks per cylinder depending on options. The total formatted capacity varies from 2,506,752 to 11,280,384 bytes, again dependent on the device and format options used.

The data encoding scheme is double frequency recording and each field is preceded by a sync word and followed by an error detection code (EDC) word and postamble. The header fields are software programmable and do not have to be numerically sequential. Note that the fourth byte of the header fields will be treated by the controller as a sector number.

When a track is formatted, 12 or 24 sectors are written beginning at the sector following the index mark. The sector headers are specified by software and are extracted from memory during the format operation. Data field will be zero filled during formatting.

Track Format

The disk track format is shown in Figure 6-17.

Sector Gap (GAP 1)

The field begins at the leading edge of a Sector Pulse and is comprised of 18 bytes of zeros.

Identifier Sync Word (SW1)

This two byte field leading the identifier field consists of the hex characters FAAA.

Sector Identifier

This is a four byte field which is formatted as shown in Figure 6-17.Platter select (bit 4 of byte 1) represents the platter (fixed or removable). The Cylinder Number is a 9 bit binary number (right justified in bytes 1 and 2) which represents

Figure 6-17. Disk Track Format

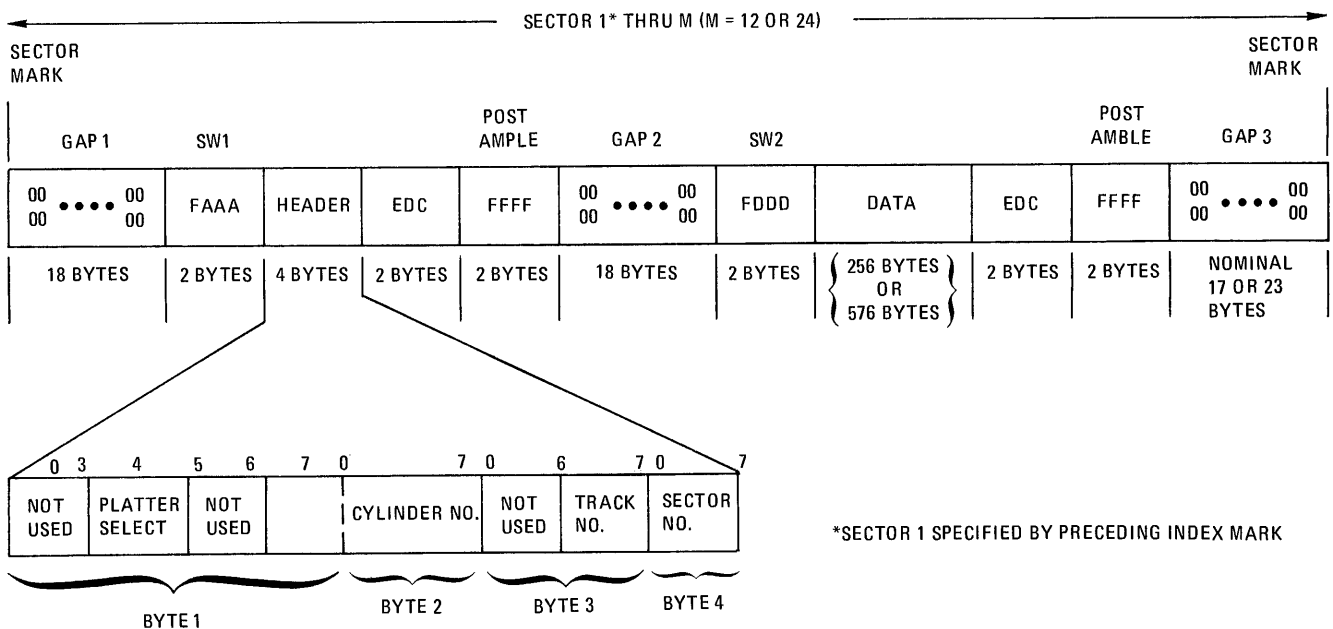the logical cylinder number from 000, for the outermost track, to 203 or 407 for the innermost track. The track number (bit 7 of byte 3) represents the upper or lower surface of the selected platter. The Sector Number is a binary number (right justified in byte 4) which represents the sector address.

Error Detection Code (EDC)

The two EDC bytes are hardware generated by use of a half add algorithm in a 16 bit register. Data and ID bytes exclusively (no sync words, postamble, or gap bytes) are used for EDC generation.

This polynomial is used for both Sector ID fields and Data fields.

Postamble

This two byte field follows the EDC bytes and consists of two bytes of all ones.

Identifier to Data Gap (GAP 2)

This field begins with the first byte after the Sector ID Postamble bytes and consists of 18 bytes of zeros. Write transitions may occur in this field as a result of an update write operation.

Data Field Sync Word (SW2)

This two byte field leading the data field consists of the hex characters FDDD.

Data Field

Data fields are always 256 or 576 bytes long. Any write operation that does not write a complete data field will result in the rest of the field being zero filled. The Format Write operation causes all the data fields on a particular track to be zero filled.

Data Field to Sector Mark Gap (GAP 3)

This field begins with the first byte after the Data postamble bytes and consists of zeros to the next sector mark. The length of this gap is dependent on the speed of the particular drive on which the medium is mounted when it is formatted or updated (nominally 17 bytes for a 256 byte data field or 23 bytes for a 576 byte data field).

Defective Track Handling

New disk media may be shipped with a minimal number of defective areas. These defective areas in conjunction with areas which may become defective during the life of the medium, are accounted for by software via a Volume Index of Defective Sectors. When a particular sector (or track) is deemed defective, allocation of space on

the disk will be made around the bad sector or track.

The controller provides no specific support for the identification or skipping of defective sectors or tracks.

Instructions

Table 6-14 lists the I/O commands to which the MSC/Cartridge Disk Device-Pac/disk units respond. A detailed description of each command follows this table.

TABLE 6-14. CARTRIDGE DISK COMMANDS

Type	Function Code	Command
Output	09 [a]	Output Address
	0D	Output Range
	0F	Offset Range
	11	Output Configuration Word A
	13	Output Configuration Word B
	03	Output Interrupt Control
	07	Output Task Word
	01	Output Control Word
Input	0C	Input Range
	0E	Input Offset Range
	10	Input Configuration Word A
	12	Input Configuration Word B
	02	Input Interrupt Control
	26	Input Device ID
	06	Input Task Word
	18	Input Status Word

[a] Function Code 09 as executed by the CP will result in execution of functions 09 and 0D.

Output Commands

Command:
Output Address

Function Code:
09

Format:

Address Bus

0	7 8	17 18	23
Module Number	Channel Number	0 0 1 0 0 1	

Data Bus
0	15
Byte Address	
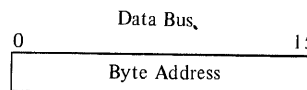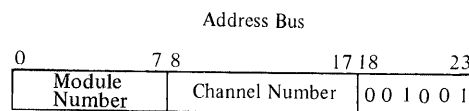
Function:
This instruction loads a 24 bit address into the address register associated with the referenced
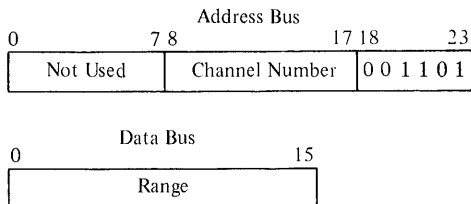
channel (device). The address refers to the starting (byte) location in main memory where the MSC will commence input or output data transfers. Bits 0-7 of the Address Bus (Module Number) are the most significant bits of the Address. The Data Bus contains the 16 least significant bits. Data transfers to or from memory will normally be on a word basis but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary.

Command:
Output Range

Function Code:
0D

Format:

Address Bus

Not Used	Channel Number	0 0 1 1 0 1

0   7 8   17 18   23

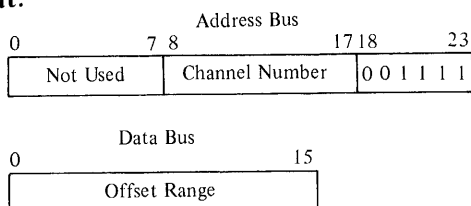Data Bus

Range

0   15

Function:
This instruction loads the Range register associated with the referenced channel. The (16 bit) quantity loaded (data bus) is the number of bytes to be transferred during the data transfer that is being set up. The number is a positive binary quantity (bit 0 must be zero) and is decremented by the MSC after each memory transfer. A range of zero will result in a premature End-of-Operation termination for any read or write command that may be subsequently issued (see Output Task Word). Any Range register residue will be applied to the next command unless reset by another Output Range Instruction.

Command:
Output Offset Range

Function Code:
0F

Format:

Address Bus

Not Used	Channel Number	0 0 1 1 1 1

0   7 8   17 18   23

Data Bus

Offset Range

0   15

Function:
This instruction loads the Output Offset Range Register associated with the referenced channel. The (16 bit) quantity loaded (data bus) is the number of bytes to be discarded from the beginning of the data transfer prior to the transfer of any data to main memory. The output range is decremented only after the offset range register is decremented to zero. The output offset range is used only in conjunction with read operations (offset range ignored for write operations) and must be set for each data transfer using an offset. The offset is a positive binary quantity and is decremented by the MSC after each byte read from the disk. Any Offset Range Register residue will be applied to the next command unless reset by another Output Offset Range Instruction.
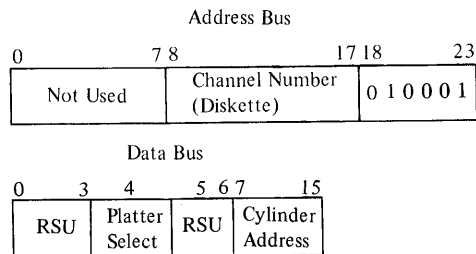
Command:
Output Configuration Word A

Function Code:
11

Format:

Address Bus

Not Used	Channel Number (Diskette)	0 1 0 0 0 1

0   7 8   17 18   23

Data Bus

RSU	Platter Select	RSU	Cylinder Address

0   3   4   5 6 7   15

Function:
This instruction loads Configuration Word A for the device corresponding to the referenced channel. The cylinder Address (bits 7-15) and Platter Select (bit 4) are used as the seek argument during seek operations. The complete word is used as the two high order bytes of a Sector ID field to be searched for during an update Read or Write operation. Bits 0-3 and bits 5-6 are reserved for software use (RSU). The maximum cylinder address permissible is 203 or 407 dependent on the device type. Bit 4 provides the platter selection address for any read or write operations. The platter selection is as follows:

Bit 4	
0	Removable media
1	Fixed media

Note that for a 200 tpi drive, selection of the fixed media when on the removable, or vice versa, will cause a 7 msec Seek to occur.

Command:
Output Configuration Word B

Function Code:
13

Format:

Address Bus

Not Used	Channel Number	0 1 0 0 1 1

(bits: 0 7 8 17 18 23)

Data Bus

RSU	Track Number	Sector Number

(bits: 0 6 7 8 15)

This instruction loads Configuration Word B for the device corresponding to the referenced channel. This word is used as the low order two bytes of a Sector ID field to be searched for during a data field Read or Write operation. Bit 7 provides the track address for any read or write operations. The track address is as follows:

Bit 7	
0	Upper surface
1	Lower surface

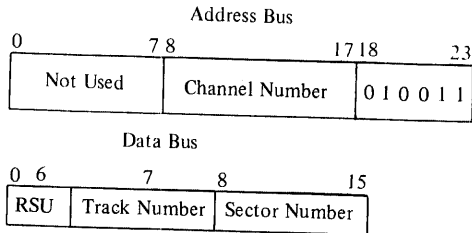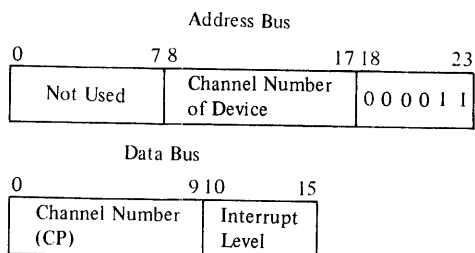The subsystem will treat bits 8 through 15 of Configuration Word B as a sector number. This number will be incremented after operating on a data field during a data field Read or Write operation. Bits 0-6 are reserved for software use (RSU).

Command:
Output Interrupt Control

Function Code:
03

Format:

Address Bus

Not Used	Channel Number of Device	0 0 0 0 1 1

(bits: 0 7 8 17 18 23)

Data Bus

Channel Number (CP)	Interrupt Level

(bits: 0 9 10 15)

This instruction loads, for the referenced device, the interrupt level and the channel number of the CP to which subsequent interrupts should be sent. The level number is a 6 bit quantity and is positioned on the data bus as illustrated above. Bits 0-9 of the data bus contain the channel number of the CP loading the interrupt level. If an interrupt level of zero is loaded, the subsystem will not generate or save interrupts for any events that occur while the interrupt level is zero. The interrupt level is set to zero whenever the subsystem is initialized.

Command:
Output Task Word

Function Code:
07

Format:

Address Bus

Not Used	Channel Number	0 0 0 1 1 1

(bits: 0 7 8 17 18 23)

Data Bus

Command Code	RFU

(bits: 0 7 8 15)

0 X X X X X X 0	–	Recalibrate
0 0 0 0 0 0 0 1	–	Seek
1 0 0 Y 0 0 0 0	–	Format Read/Write
1 0 0 Y 0 0 0 1	–	Data Field Read/Write
1 0 0 Y 0 0 1 1	–	Diagnostic Read/Write
1 1 0 0 0 0 0 0	–	Wrap Around Read/Write
1 0 0 Y 0 1 0 0	–	Format Read ID

Y = 0 { Fixed sector length = 256 bytes

1 { Fixed sector length = 576 bytes

This instruction outputs a Task Word to the referenced channel. The coding bits 0-7, illustrated above, represent the operations that are to be performed. When this instruction is accepted, the channel enters the Busy state and execution of the indicated task is immediately begun. All address, range and configuration information must be loaded prior to execution of this instruction. The direction of data transfer is indicated in the low order bit of the most recent output address instruction. For example, if the Data Field encoding of the Task Word is received when a "Read" channel number is indicated, then a Read Data command will be executed. Note that track selection (which includes the platter and

surface) is performed for each media data transfer command prior to initiation of the data transfer and is based on the current contents of configuration words A and B.

- Recalibrate — The Recalibrate command causes the channel to move the device's positioner to cylinder zero and reset the "Seek Timeout" line on the device interface. This instruction is intended as an Initialization command to guarantee that the positioner location information in the controller is correct and that the device faults are cleared. Completion of the recalibration operation by the device will result in the generation of an appropriate interrupt.

- Seek — The Seek command in the Task Word causes the channel to move the device's positioner to the cylinder and selects the platter indicated in Configuration Word A. If the cylinder specified is greater than 203 or 407 (depending on device) or an error occurs during positioner movement, then an error bit will be set in the Status Word. Completion of a positioning operation (whether or not any physical movement occurred) by the device will result in the generation of an appropriate interrupt.

- Format Read — The Format Read command causes the channel to read all Identifier (ID) and data fields on a track beginning with the first sector after index and in the order in which they are recorded. Data will be transferred to memory beginning at the memory location specified in the subsystems memory address register (after any offset has been exhausted). This address will be the address loaded by the most recent Output Address instruction if no data transfer has occurred since that instruction was executed. If one or more data transfer operations has been executed since the last Output Address instruction, then the starting memory address used for this operation will be the byte address immediately following the end of the most recent data transfer executed for this device (either Read or Write).

If Bit 6 of the command code is a one, then the EDC word of any Sector Identifier read will be ignored. If bit 6 of the command code is a zero, then the EDC word of any Sector Identifier read will be checked.

Data will be transferred until a read error occurs (except as noted for bit 6), the range is satisfied, or the entire track is read (index is detected).

Normal range for this command (to read one complete track) is:

- $R = (4 + 256) \times 24 = 6240$ bytes (for 256 byte sectors)

or

- $R = (4 + 576) \times 12 = 6960$ bytes (for 576 byte sectors)

where:

    4 = ID
    256/576 = Data
    24/12 = Sectors

If this command is terminated due to end of track before the range is satisifed, the residual range will be available via the Input Range command (see Input Range). A read error in any field (except as previously noted for bit 6 of the command code = 1) will cause the operation to be terminated with the Read Error bit set in the Status Word (bit 4). The Sector ID field in Configuration Word B will point to the record in error. The field in error can be determined through examination of the residual range (if a read error is detected in an ID field the range will have been decremented for the ID field only).

If the required transfer rate is not maintained on the Bus (156.25 KW/S), the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

If the range register is zero when this command is received, the Task will be immediately terminated (End-of-Operation). No data will be read or transferred. Track selection for the operation is based on the current contents of the Track Address of Configuration Words A and B.

- Format Read ID — The Format Read ID command is identical to the Format Read command except that only the ID's of each sector are transferred to memory.

Normal range for this command (to read one complete track) is:

- $R = 4 \times 24 = 96$ bytes (for 256 byte sectors)

or

- R = 4 x 12 = 48 bytes (for 576 byte sectors)

where

4 = number bytes in ID
24/12 = number of sectors per track.

- Format Write — The Format Write command causes the channel to format the track which is positioned under the Read/Write head specified by Configuration Words A and B when this command is received. Twelve or twenty-four (as specified by bit 3 of the task word) equal length sectors will be written starting at index. The Sector ID fields will be read from memory beginning with the memory location specified in the sub-system's memory address register.

Data fields will be written with normal data field Address Marks and will be zero filled by the MSC.

The range to format one complete track is:

- R = 4 x 24 = 96 bytes (for 256 byte sectors)

    or

- R = 4 x 12 = 48 bytes (for 576 byte sectors)

If a range other than that specified is sent for a format write, the resulting track format is unspecified.

If the range register is zero when this command is received, the Task will be immediately terminated (End-of-Operation). No data will be written.

If the Sector ID data cannot be read from memory at a sufficient rate, then the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

- Read Data — The Read Data command causes the channel to locate the sector defined by the Sector ID image loaded in Configuration Words A and B and begin to transfer the data field of (at least) that sector to main memory. Data will be transferred to memory beginning with the memory location specified in the subsystems memory address register after any offset has been exhausted (see Format Read) and will continue until the range is satisfied. When the transfer of the first specified sector data

field is completed (without error), the Sector Number field of Configuration Word B will be incremented. If the initial range is greater than 256 (or 576 if 576 byte sectors are specified) then the sector on that track represented by the updated contents of Configuration Words A and B (A is unchanged) will be located and data transfer will continue with the new sector's data field. This operation will continue until either the range is satisfied, a read error occurs, or the record specified by Configuration Words A and B cannot be located on the track (as indicated by the detection of two index marks without a successful compare). If the specified record cannot be located, then an unsuccessful search will be posted in the Status Word (bit 7).

Track selection for the operation is based on the current contents of the Track Address of Configuration Word A and B.

If a read error is encountered in a data field, the operation will be terminated and the Read Error bit in the Status Word will be set (bit 4). The Sector Number field of Configuration Word B will contain the address of the record in error. If a read error is encountered in an ID field, a mis-compare result will be assumed and the search will continue. In this case the Read Error bit will be posted in the Status Word so that if the desired record is never located the operation will be terminated with both the Unsuccessful Search bit and Read Error bit posted in the Status Word indicating that the reason for the miscompare could be a read error in the Sector ID. If the search is eventually successful, the Read Error bit in the Status Word will be reset.

If this command is terminated before the range is satisfied, the residual range will be available via the Input Range command (see Input Range). If the range register is zero when this command is received, the Task will be immediately terminated (End-of-Operation). No data will be read or transferred.

If the required transfer rate is not maintained on the Bus (156.25 KW/S), then the operation will be terminated and, the Overrun/Underrun bit will be set in the Status Word (bit 2).

- Write Data — The Write Data command causes the channel to locate the sector

defined by the Sector ID image loaded in Configuration Words A and B and to rewrite the data field of at least that sector. The data will be read from memory beginning with the memory location specified in the subsystem's memory address register (see Format Read). Rewritten data fields will be preceded by normal data field sync words (see Figure 6-17).

When the transfer of the specified sector is completed, the Sector Number field of Configuration Word B will be incremented. If the range is less than 256 or 576, the data field will be zero filled. If the range is greater than 256 or 576, the sector represented by the updated contents of Configuration Words A and B (A is unchanged) will be located and the data field rewritten (preceded by a normal data field sync word). This operation will continue until either the range is satisfied or the record specified by Configuration Words A and B cannot be located on the track (as indicated by the detection of two index marks without a successful ID field compare). If the latter event occurs, Unsuccessful Search will be posted in the Status Word (bit 7).

If two or more records are to be updated with a single Write Data command, they will be written in sequence without the loss of a revolution.

If a read error is encountered in an ID field, that sector will be bypassed and the search will continue. In this case, the Read Error bit will be posted in the Status Word so that if the desired record is never located, the operation will be terminated with both the Unsuccessful Search bit and the Read Error bit posted in the Status Word indicating that the reason for the unsuccessful search could be a read error in the Sector ID. If the search is eventually successful, the Read Error bit in the Status Word will be reset.

If this command is terminated before the range is satisfied, the residual range will be available via the Input Range command (see Input Range). If the range register is zero when this command is received, the Task will be immediately terminated (End-of-Operation). No data will be written.

If the required transfer rate is not maintained on the Bus (156.25 KW/S), the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2).

Track selection for the operation is based on the current contents of the Track Address of Configuration Words A and B.

- Write Diagnostic — The Write Diagnostic command causes the channel to perform as if the Write Data command was specified except that invalid EDC characters will be written at the end of each data field updated (the EDC characters will always be zero). Note that the data written in the data fields will be read from memory and normal data field sync words will be written (for all fields written by this command).

Track selection for the operation is based on the current contents of the Track Address of Configuration Word A.

- Read Diagnostic — The Read Diagnostic command causes the channel to read everything on a track (including gaps, sync words, ID and data fields, and EDC bytes) beginning with the first sync word after the next sector pulse detected and ending at the record index pulse. Meaningful operation of this command can only be guaranteed on tracks which have not been updated since the last format operation (updated records may contain write splice discontinuities). No EDC checks will be done. Data will be transferred until the range is satisfied or the second index pulse is detected. Normal range for this command (to read one complete track) is:

$$R = [(312.5K \text{ Bytes/sec}/(2400RPM)] (1.02)$$
$$7968 \text{ bytes/track}$$

If this command is terminated due to end of track before the range is satisfied, the residual range will be available via the Input Range Command (see Input Range).

If the required transfer rate is not maintained on the Bus (156.25 KW/S), the operation will be terminated and the Overrun/Underrun bit will be set in the Status Word (bit 2). Track selection for the operation is based on the current contents of the Track Address of Configuration Words A and B.

- Wraparound Read/Write — During a Wraparound Write command, the channel will read 1-96 bytes from memory (at the Address specified in the subsystem's memory address register) and transfer the bytes to the Cartridge Disk Device-Pac.

When a Wraparound Read command is received (immediately following a Wraparound Write) the bytes loaded into the Device-Pac buffer by the previous Wraparound Write command, will be returned to main memory at the address specified in the subsystem's memory address register. The bytes returned during this operation should be the same as the bytes supplied by software in the preceding Wraparound Write command.

A range of 1-96 should be specified for these commands. If a zero range is specified, the command will be immediately terminated (without being executed). If a range greater than 96 is specified a residual range will be present at termination.
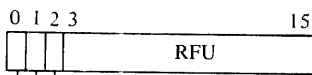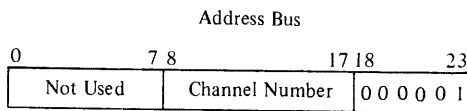
Command:
  Output Control Word

Function Code:
  01

Format:

Address Bus

```
0           7 8              17 18        23
 ┌──────────┬──────────────┬─────────────┐
 │ Not Used │Channel Number│ 0 0 0 0 0 1 │
 └──────────┴──────────────┴─────────────┘
```

```
0 1 2 3                      15
 ┌┬┬┬──────────────────────────┐
 ││││          RFU             │
 └┴┴┴──────────────────────────┘
  │ │ │
  1 0 0 ── Initialize
  0 1 0 ── Stop I/O
  0 0 1 ── Test Mode
```

Function:
  This instruction loads a Control Word into the referenced channel. This command will be unconditionally accepted by the channel regardless of its Busy status.

- Initialize — This command will cause the MSC to reset to the same state that it enters after power up. When an initialize command is received by the MSC all of its channels are initialized (regardless of which channel the command was received over). A Recalibrate will be executed on all cartridge disk drives.

  Operations that are in progress in the MSC at the time of the Initialization will be abruptly terminated and all registers will be initial-

ized. No information about the terminated operations will be retained and no interrupts for the operations will be generated. The interrupt level for all channels will be set to Zero (interrupts blocked).

- Stop I/O — This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress, it will not be completed nor will any error checking be done. An Interrupt will be generated for the operation terminated by this command as if the operation had come to a normal ending point. Status, Address and Range information, present in the MSC when this command is received, will be retained. Note that execution of this command may result in invalid data on the media (if a write operation was in progress) or a device fault (if a seek operation had been initiated and not completed prior to a subsequent operation).

- Test Mode — When an Output Control Word command is received with the Test Mode bit on, the MSC will enter Test Mode. Once the MSC is in Test Mode, specific diagnostic type operations may be initiated providing different levels of wraparound within the MSC and the Cartridge Disk Device-Pac.

  Test Mode operates on an entire MSC and, therefore, precludes normal usage of other devices on the MSC at the same time. Normal mode is resumed when a "reset test mode" microinstruction is executed or when Master Clear is activated on the Bus.

Input Commands

Command:
  Input Range
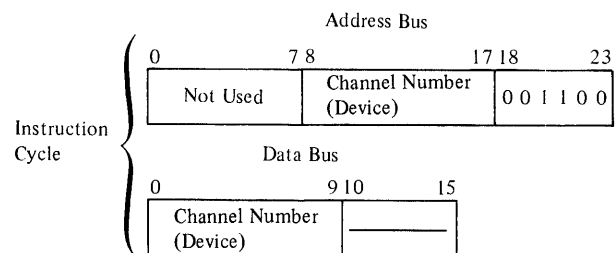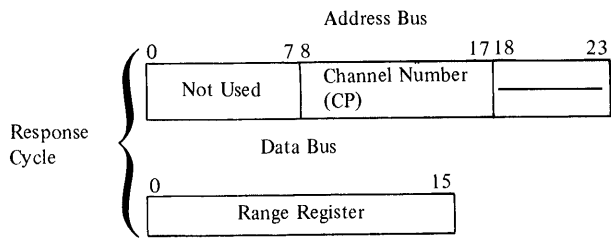
Function Code:
  0 C

Format:

Address Bus

```
            0           7 8                 17 18        23
           ┌──────────┬──────────────────┬─────────────┐
Instruction│ Not Used │ Channel Number   │ 0 0 1 1 0 0 │
Cycle      │          │ (Device)         │             │
           └──────────┴──────────────────┴─────────────┘
                        Data Bus
            0               9 10        15
           ┌──────────────┬─────────────┐
           │Channel Number│ ─────────── │
           │(Device)      │             │
           └──────────────┴─────────────┘
```

Response Cycle

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)		

Data Bus

0	15
Range Register	

Function:

This instruction causes the current contents of the referenced channel's Range Register to be transferred to the requesting channel.

During the Response Cycle (Second Half Read), the MSC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction Cycle.

After the completion of a data transfer operation, the contents of the Range Register reflect the status of that transfer with respect to the physical sector(s) read.

- If the contents is a positive value greater than zero, the length of the physical sector(s) was less than the sum of the original offset range and range.
- If the contents is zero, the length of the physical sector(s) was equal to or greater than the sum of the original offset range and range.

Command:
Input Offset Range

Function Code:
0E

Format:

Instruction Cycle

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Device)	0 0 1 1 1 0	

Data Bus

0	9 10	15
Channel Number		

Response Cycle

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)		

Data Bus

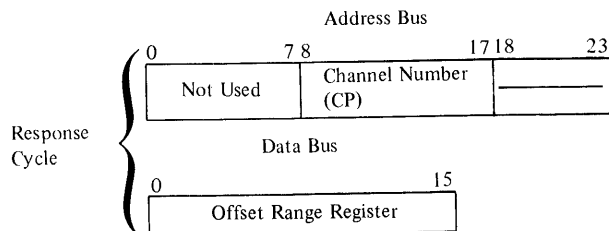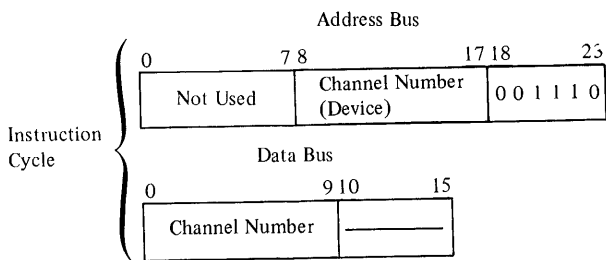| 0	15
Offset Range Register	

Function:

This instruction causes the current contents of the referenced channel's Offset Range Register to be transferred to the requesting channel.

During the Response Cycle (Second Half Read), the MSC will retain in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction Cycle.

After completion of data transfer operation, the contents of the Offset Range Register reflect the status of that transfer with respect to the physical sector(s) read.

- If the contents is a positive value greater than zero, the length of the physical sector(s) was less than the original offset range.
- If the contents is zero, the length of the physical sector(s) was equal to or greater than the original offset range.

Command:
Input Configuration Word A

Function Code:
10

Format:

Instruction Cycle

Address Bus

0	7 8	17 18	23	
Not Used	Channel Number (Device)	0 1 0 0 0 0	"A"
		0 1 0 0 1 0	"B"

Data Bus

0	9 10	15
Channel Number (CP)		

Response Cycle

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)		

Data Bus

0	15
Configuration Word A (B)	

Function:

This instuction causes the channel's Configuration Word A (B) to be transferred to the requesting channel.

During the Response cycle (Second Half Read) the MSC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle.

Command:
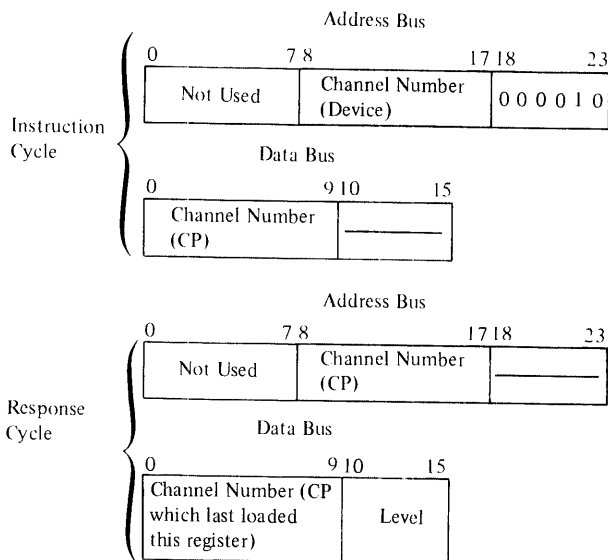Input Configuration Word B

Function Code:
12

Format:
See "Input Configuration Word A"

Function:
See "Input Configuration Word A"

Command:
Input Interrupt Control

Function Code:
02

Format:

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Device)	0 0 0 0 1 0	

Instruction Cycle

Data Bus

0	9 10	15
Channel Number (CP)	———	

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)	———	

Response Cycle

Data Bus

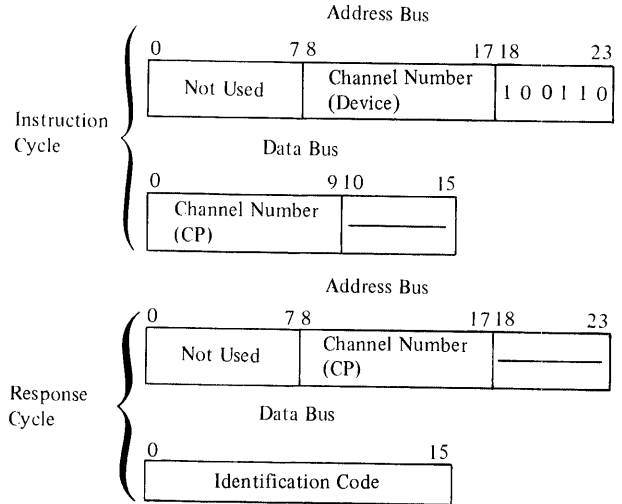| 0	9 10	15
Channel Number (CP which last loaded this register)	Level	

Function:
This instruction causes the channel's interrupt level to be transferred to the requesting channel. The level value will be placed on Data Bus bits 10 through 15 (see above) with bit 15 as the least significant bit. This quantity is the value previously received in the Output Interrupt Control instruction, or, a default value of 00. The default value is the interrupt level assumed by the channel when initialized. Note that the channel number returned in bits 0-9 of the Data Bus might be different than the channel number of the CP executing this instruction if more than one CP is attached to the Bus.

During the Response cycle (Second Half Read) the MSC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the instruction cycle.

Command:
Input Device ID

Function Code:
26

Format:

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Device)	1 0 0 1 1 0	

Instruction Cycle

Data Bus

0	9 10	15
Channel Number (CP)	———	

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)	———	

Response Cycle

Data Bus

0	15
Identification Code	

Function:
This instruction will cause the referenced channel to transfer its identification code to the requesting channel. Depending on the device accessed, one of the following codes will be returned.

Code (Hex)	Model
2330	100 tpi, no fixed disk (CDU9101)
2331	100 tpi, with fixed disk (CDU9102)
2332	200 tpi, no fixed disk (CDU9103)
2334	200 tpi, with fixed disk (CDU9104)

During the response cycle (Second Half Read) the MSC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the instruction cycle.

Command:
Input Task Word

Function Code:
06

Format:

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Device)	0 0 0 1 1 0	

Instruction Cycle

Data Bus

0	9 10	15
Channel Number (CP)	————	

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)	————	

Response Cycle

Data Bus

0	15
Task Word	

Function:

This instruction causes the Task Word of the referenced channel to be transferred to the requesting channel. The Task Word transferred will contain the code for the last operation executed by the channel (unless an Initialize has occurred).
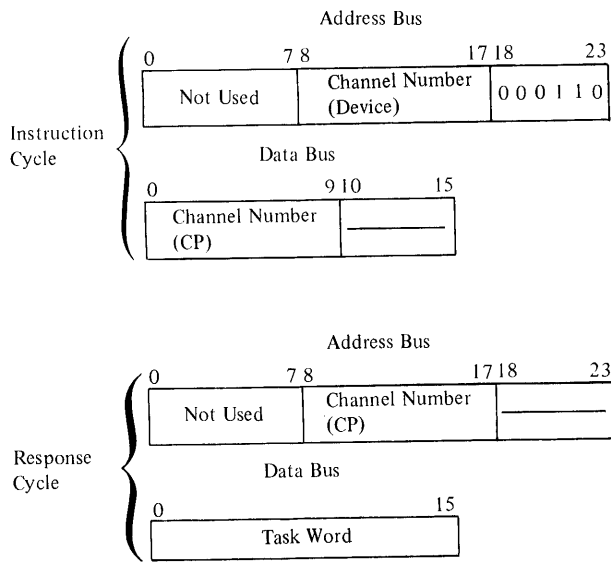
During the Response cycle (Second Half Read) the MSC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle.

Command:
Input Status Word

Function Code:
18

Format:

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (Device)	0 1 1 0 0 0	

Instruction Cycle

Data Bus

0	9 10	15
Channel Number (CP)	————	

Address Bus

0	7 8	17 18	23
Not Used	Channel Number (CP)	————	

Response Cycle

Data Bus

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

0	Device Ready
1	Attention
2	Overrun/Underrun
3	Write Protection Error
4	Read Error
5	Illegal Seek
6	Missed Data Sync
7	Unsuccessful Search
8	Missing Clock Pulse
9	Missing Sector Pulse
10	Seek Error
11	Not Used
12	Corrected Memory Error
13	Non-Existent Resource
14	Bus Parity Error
15	Uncorrected Memory Error

Function:

This instruction causes the referenced channel's Status Word to be transferred to the requesting channel.

During the Response cycle (Second Half Read) the MSC will return in bits 8-23 of the Address Bus, the same data that was received in bits 0-15 of the Data Bus during the Instruction cycle. See also Table 6-15.
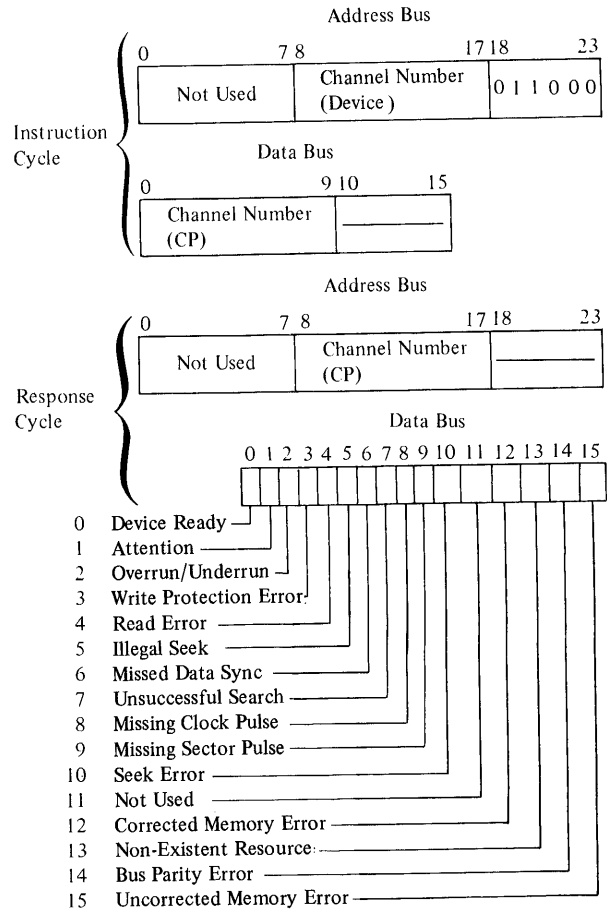
TABLE 6-15. STATUS BIT DEFINITIONS – CARTRIDGE DISK

Status Condition	Bit	Definition	Reset By
Device Ready	0	This bit indicates that the device is online with the medium loaded and that no further manual intervention is required to place it under program control. Note that a change of state of this bit will cause the Attention bit (bit 1) to be set resulting in an interrupt (if the interrupt level is non-zero).	A change in condition.
Attention	1	This indicator will be set whenever the Device Ready bit (bit 0 of the status word) changed state. Any change of operational status of the device (e.g., load/unload of media) will be indicated to software in this way.	Output Control Word,[1] Input Status Word, Output Task Word, or Master Clear on the bus.

[1] Initialize encoding only

TABLE 6-15(cont). STATUS BIT DEFINITIONS — CARTRIDGE DISK

Status Condition	Bit	Definition	Reset By
		Whenever the Attention bit is set an interrupt is attempted (if the interrupt level is non-zero). If a previously initiated operation is in progress when a device state change is sensed the resultant interrupt (with the Attention bit set) will serve as notification of both the end of the operation and the device state change.	
Overrun/Underrun	2	This bit is set during a Read or Write operation when the data transfer to/from main memory cannot be maintained at a high enough rate (156 KW/S during field transfers in word mode). Either data was lost on input because of failure to keep up with device demands or data was unavailable on output when required by the device.	Output Control Word,[1] Output Task Word, or Master Clear on the bus.
Write Protection Error	3	This bit will be set if an attempt is made to perform any Write operation on a protected surface (i.e., Write Protect is set on the device). Note that operator intervention is required to reset the Write Protect condition of the device.	Same as preceding bit.
Read Error	4	This bit is set during any Read operation if the EDC Word at the end of a field disagrees with the EDC Word calculated while reading the field.	Same as preceding bit.
Illegal Seek (100 tpi device only)	5	This bit is set if bit 7 of Configuration Word A is equal to a one during a Seek Command execution.	Same as preceding bit.
Missed Data Sync	6	This bit will be set if, after a Sector ID has been detected during a Read operation, the corresponding data field is not detected or if during a Format Read two consecutive Data field (or two consecutive ID field) address marks are detected (indicating that a field was missed).	Same as preceding bit.
Unsuccessful Search	7	This bit is set during a non-format Read or Write operation for which the Sector.ID specified in Configuration Words A and B cannot be located on the Track.	Same as preceding bit.
Missing Clock Pulse	8	This bit will be set if the controller detects a missing clock pulse during write operations. Note that a missing clock pulse during a read operation will result in a Read Error.	Same as preceding bit.
Missing Sector Pulse	9	This bit will be set if the controller detects missing sector pulses for a period of 1.5 msec. This normally indicates that one of the fixed surfaces (tracks 2 or 3) have been selected on a device which has no fixed platter.	Same as preceding bit.

[1] Initialize encoding only.

TABLE 6-15(cont). STATUS BIT DEFINITIONS – CARTRIDGE DISK

Status Condition	Bit	Definition	Reset By
Seek Error	10	This bit is set during a seek operation if the MSC receives a seek error indication from the device. This condition occurs if the device does not successfully complete a seek operation, or if an attempt is made to seek beyond the cylinder limits.	Output Control Word,[1] Recalibrate, or Master Clear on the bus.
Corrected Memory Error	12	This bit indicates that during execution of the previous operation Main Memory detected and corrected a memory read error. The data that was delivered to the MSC was assumed to be correct.	Output Control Word,[1] Output Task Word, or Master Clear on the bus.
Non-Existent Resource	13	This bit is set whenever the MSC attempts a Write or Read request Bus cycle and receives a NAK response.	Output Control Word,[1] Output Task Word, or Master Clear on the bus.
Bus Parity Error	14	This bit will always be zero (not supported by the MSC).	--
Uncorrected Memory Error	15	This bit indicates that during execution of the previous operation Main Memory detected a memory read error which the EDAC algorithm could not correct. The data that was delivered to the MSC was incorrect. Occurrence of this condition will not cause termination of the operation in progress (may result in bad data written on the medium).	Output Control Word,[1] Output Task Word, or Master Clear on the bus.

[1] Initialize encoding only

Specifications

Capacity

Type	CDU9101	CDU9102	CDU9103	CDU9104
Density	Low	Low	High	High
Media	Removable	Removable and Fixed	Removable	Removable and Fixed
Bytes/Sector	256/576	256/576	256/576	256/576
Sectors/Track	24/12	24/12	24/12	24/12
Bytes/Track	6,144/6,912	6,144/6,912	6,144/6,912	6,144/6,912
Tracks/Cylinder	2	4	2	4
Bytes/Cylinder	12,288/13,824	24,576/27,648	12,288/13,824	24,576/27,648
Cylinders/Unit	204	204	408	408
Bytes/Unit	2.5/2.8 MB	5.0/5.6 MB	5.0/5.6 MB	10.0/11.2 MB
Units/Controller	4	4	4	4
Bytes/Controller	10.0/11.2 MB	20.0/22.5 MB	20.0/22.5 MB	40.1/45.1 MB

Simultaneity

During data transfer on one unit, simultaneous seek operations can be performed on all other units attached to the same controller.

Speed/Rates

AVERAGE LATENCY (ROTATIONAL): 12.5 ms SEEK TIMES: Same Cylinder – 0; Track to Track – 9 ms; Average Random – 35 ms: Maxi-

mum (408 tracks) – 60 ms; Transfer Rate – 2.5 million bits/second; 312K bytes/second; 156K words/second.

Controller

MSC9101 controls up to four disk units of the same density.

Device Interface

A single Device-Pac (CDM9101) interfaces up to four disk units.

Disk Pack

A Honeywell Type M4024 cartridge disk (or equivalent) is used for either the high- or low-density units.

Physical Dimensions

Height:	8.75 inches (24 cm)
Width:	17.75 inches (45 cm)
Depth:	30.0 inches (76.2 cm)
Weight:	84 pounds (40 kg)
(with pack)	

Power

Voltage:	120/220 Vac +10%, -15%; 240 Vac +6%, -15%
Frequency:	60/50 Hz ±0.5 Hz

SERIAL PRINTERS

The Types PRU9101 and 9102 Serial Printers are self-contained, table-top sized printers designed for low-cost printing requirements (Figure 6-18). The printers have 64-and 96-ASCII code character sets, respectively. Both operate at 165 characters per second and print at line speeds of 60 lines per minute (lpm) for 132 chars./line and 200 lpm for 20-30 chars./line.

The printers interface with the 6/30 Models by means of a single-board Multiple Device Controller (MDC9101), a Printer Device-Pac (PRM-9101), and a 50-foot cable. The printers can be made self-standing via Option PRF9101, the serial printer pedestal.

Features

- Upper/lower case print capability with PRU9102
- Separate offline test mode for easy maintenance
- Line speeds of 60 lpm at 132 characters per line; 200 lpm at 20-30 chars./line
- Original and up to four carbon copies
- Vertical forms tape permits various form sizes
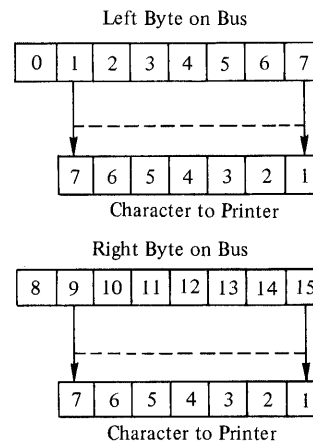
Operation

Data to the serial printer must be in standard ASCII 7-bit format. A maximum of 132 characters per line and only one line at a time can be printed per operation. All data transfers are under DMA (Direct Memory Access) control.

Spacing to top-of-form and testing for end-of-form is controlled via holes punched into a paper tape. The operator may, therefore, change the spacing by simply punching a new paper tape.

Data Handling

The range of the data buffer in memory is expressed in bytes and should be equal to or less than one print line. The number of bytes transferred may be even or odd and the starting address of the buffer may be on any byte boundary. The MDC will fetch words from memory but will send only the specified bytes to the printer.

The data to the printer will correspond to the bus data in the following way:

Left Byte on Bus

0	1	2	3	4	5	6	7

7	6	5	4	3	2	1

Character to Printer

Right Byte on Bus

8	9	10	11	12	13	14	15

7	6	5	4	3	2	1

Character to Printer

The eighth bit (bit 0 or 8 on the bus) is a "don't care" bit so that the same character will be printed regardless of the state of that bit.

The 64- and 96-character ASCII sets are shown in Table 6-16. The MDC/Printer will perform limited code translation on the data. Figure 6-19 is a diagram of the data manipulation by the Device-Pac. The data buffer specified by the software will be code converted so that it will be printed regardless of the number of printable characters supported by the printer (64 or 96). Control commands are supplied by the software driver separately from the data buffer and are inserted in the data stream after the code translation has taken place.

Code translation is limited to bit 6 (bus bit 2 or 10) and is as follows:

64 Character Set	if b7, b6 = 00, set to 01
	if b7, b6 = 11, set to 10
96 Character Set	if b7, b6 = 00, set to 01
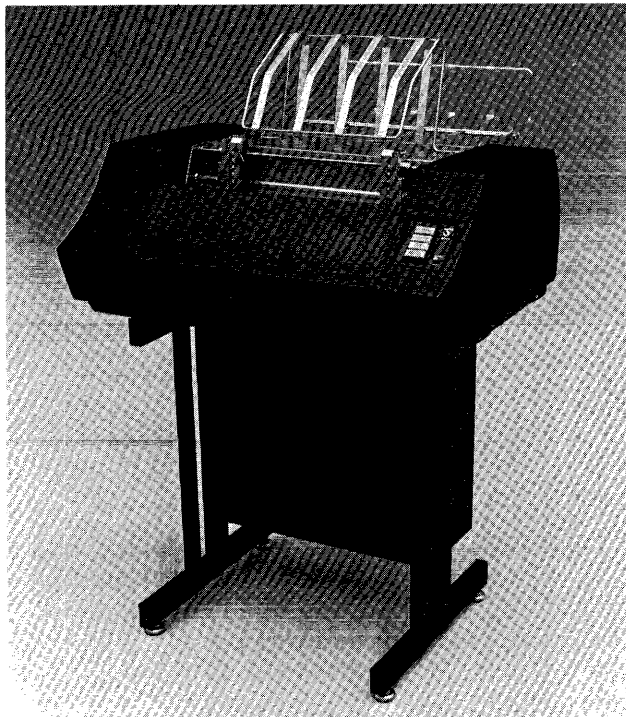
Figure 6-18. PRU9101/9102 Serial Printers

TABLE 6-16. 96 CHARACTER ASCII SET

B4	B3	B2	B1		B8 →	0	0	0	0	0	0	0	0
					B7	0	0	0	0	1	1	1	1
					B6	0	0	1	1	0	0	1	1
					B5	0	1	0	1	0	1	0	1
				Col / Row		0	1	2	3	4	5	6	7
0	0	0	0		0	Space	0	Space	0	@	P	'	p
0	0	0	1		1	!	1	!	1	A	Q	a	q
0	0	1	0		2	"	2	"	2	B	R	b	r
0	0	1	1		3	#	3	#	3	C	S	c	s
0	1	0	0		4	$	4	$	4	D	T	d	t
0	1	0	1		5	%	5	%	5	E	U	e	u
0	1	1	0		6	&	6	&	6	F	V	f	v
0	1	1	1		7	'	7	'	7	G	W	g	w
1	0	0	0		8	(	8	(	8	H	X	h	x
1	0	0	1		9	)	9	)	9	I	Y	i	y
1	0	1	0		A	*	:	*	:	J	Z	j	z
1	0	1	1		B	+	;	+	;	K	[	k	{
1	1	0	0		C	,	<	,	<	L	\	l	|
1	1	0	1		D	-	=	-	=	M	]	m	}
1	1	1	0		E	.	>	.	>	N	∧	n	∧
1	1	1	1		F	/	?	/	?	O	-	o	Note

NOTE: Serial Printer (PRU9102) prints this as a space. Line Printers (PRU9103/9105) prints this as a box.
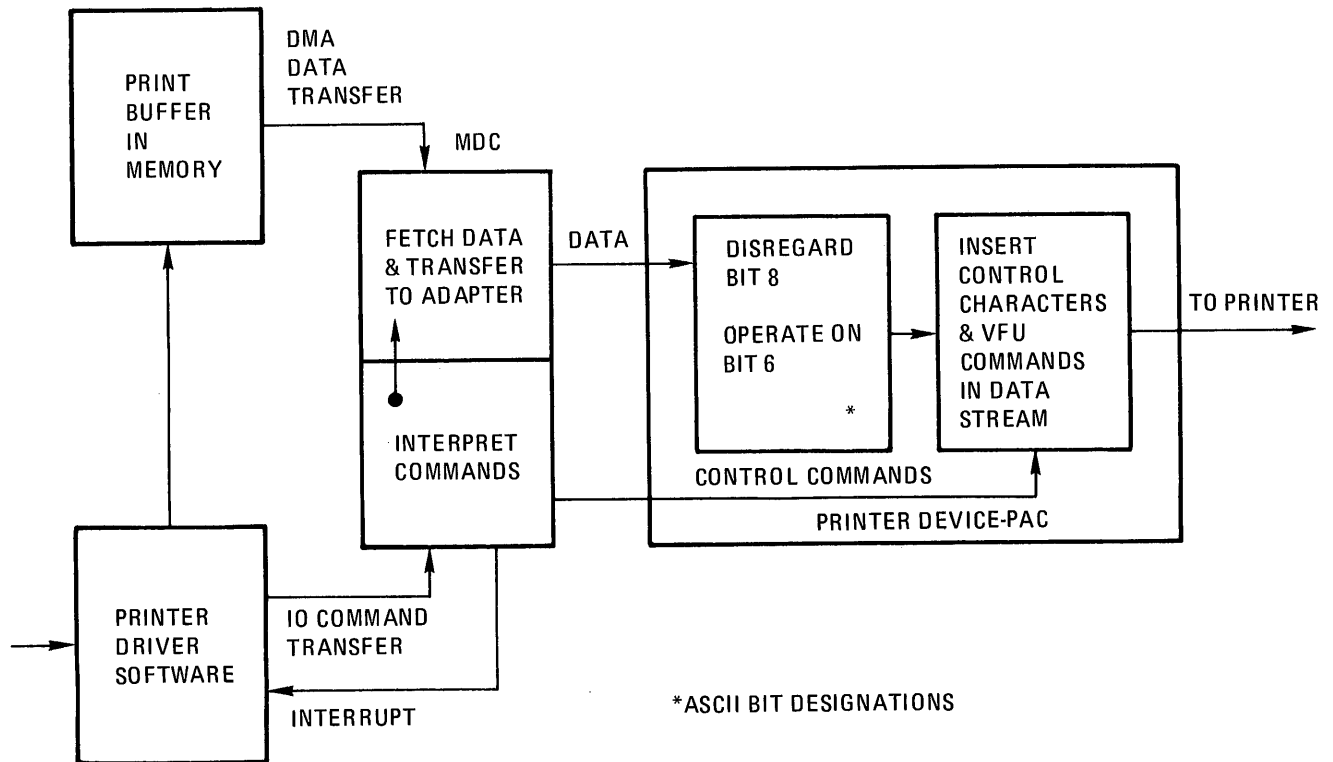
Figure 6-19. Data Manipulation of Printer Device-Pac

Instructions

Table 6-17 lists the I/O commands to which the MDC/printer Device-Pac/printers respond. A detailed description of each command follows this table.

TABLE 6-17. SERIAL PRINTER COMMANDS

Type	Function Code	Command
Output	05	Output Interrupt Control
	01	Output Control
	07	Output Task Word
	09	Output Address and Range
Input	04	Input Interrupt Control
	06	Input Task Word
	08	Input Memory Byte Address
	0A	Input Memory Module Address
	0C	Input Range
	18	Input Status Word 1
	1A	Input Status Word 2
	26	Input Device ID

NOTE: The instructions and programming information presented in this section also pertains to users of the PRU9103/9104/9105/9106 Line Printers.

Output Commands

Command:
Output Interrupt Control

Function Code:
05

Format:
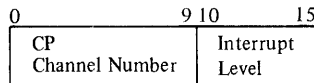
```
0                9 10        15
┌────────────────┬───────────┐
│ CP             │ Interrupt │
│ Channel Number │ Level     │
└────────────────┴───────────┘
```

Function:
Loads a 16-bit word into the interrupt control register with the information necessary for generating an interrupt, i.e., the interrupt level and which CP the interrupt is to be issued to.

Command:
Output Control

Function Code:
01

Format:

```
0 1 2 3 4                          15
┌─┬─┬─┬─┬─┬──────────────────────────┐
│ │ │ │ │ │        Not Used          │
└─┴─┴─┴─┴─┴──────────────────────────┘
 1 0 0 0 0  −  Initialize
 0 1 0 0 0  −  Stop I/O
 0 0 1 0 0  −  Test Mode
 0 0 0 1 0  −  Freeze Address
```

Function:
Loads a 16-bit control word into the referenced channel and will be accepted unconditionally regardless of any channel busy status. The channel may respond with a WAIT, but never with a NAK. The individual bits will cause the following specific action to occur:

- Initialize
  - Causes the MDC to run its resident logic test
  - Clears all MDC Device-Pacs
  - Operates on all channels of MDC
  - Makes all channels of MDC non-busy
  - Blocks interrupts
- Stop I/O
  - Makes channel non-busy (causes interrupt if enabled)
  - Does not affect other channels
  - Causes channel to terminate its I/O operation and update status
- Freeze Address
  - Prevents the MDC from modifying its DMA address register during operation. The printer works normally in all respects except that the entire transfer takes place from the same memory location.
- Test Mode
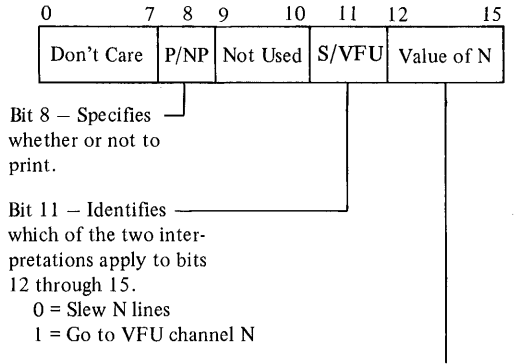 - See paragraph entitled "Test Mode".

Command:
Output Task Word

Function Code:
07

Format:

```
0          7 8  9    10  11  12        15
 _____
| Don't Care |P/NP| Not Used |S/VFU| Value of N |
 _____
```

Bit 8 — Specifies
whether or not to
print.

Bit 11 — Identifies
which of the two inter-
pretations apply to bits
12 through 15.
   0 = Slew N lines
   1 = Go to VFU channel N

Bits 12 through 15 specify a number which may be either a
VFU channel or the number of lines to be spaced. Bit 11
identifies which of the two interpretations apply to bits
12 through 15. The maximum value of N is 15 for a spacing
operation. For a VFU operation, the maximum
value of N is 12. Printers without VFU will go to
top of form by being commanded to go to VFU
channel 0.

The device ID number can be used to determine which of
the printers is installed. In the case a VFU command is
issued, where a VFU is not installed or where the VFU
number is too large, the VFU command will be ignored
and the data will be printed with a single line space.

Function:
Outputs a word that determines the specific
printer action to be performed.

Command:
Output Address and Range

Function Code:
09

Format:

```
0                                    23
 _____
|          Address Transfer             |
 _____
```

```
0                      15
 _____
|     Range Transfer      |
 _____
```

Function:
The IOLD command when executed by the
processor creates two bus transfers to the MDC.
The first is the 24-bit address transfer and the
second is the 16-bit range transfer. To the MDC,
these are two separate and distinct bus transfers
with two separate and distinct function codes of
09 for the address transfer and OD for the range
transfer. The programmer need only specify the
first function code and the processor hardware/
firmware will automatically calculate the second
function code (by adding 04 to it).

- *Address Transfer* — A 24 bit quantity
  transferred to the MDC to be used as the
  starting byte address of the data record in
  memory which is to be transferred.
- *Range Transfer* — A 16 bit quantity trans-
  ferred to the MDC to be used as the byte
  range count of the data record in memory
  which is to be transferred. Range is specified
  as a two's complement integer which must
  be positive for the MDC. Therefore, for the
  MDC, Range is:

$$1 \leqslant r \leqslant 2^{15} - 1$$

Range should be restricted to the line length of
the printer attached. The reaction of the printers
to a buffer in excess of this is as follows:

1. Line Printer — Characters in excess of 136
   are output by the printer Device-Pac, but
   discarded by the printer.
2. Serial Printer — Characters in excess of 132
   overprint starting with the first column.

The range transfer includes the implicit command
Start I/O and causes the MDC to start print and
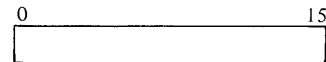to go Busy.

Input Commands

Command:
Input Interrupt Control

Function Code:
04

Format:

```
0                              15
 _____
|                               |
 _____
```

Function:
Causes the channel to place the contents of its
interrupt control register on the data bus.

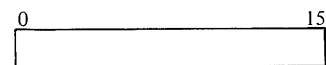**Command:**
Input Task Word

Function Code:
06

Format:

```
0                              15
 _____
|                               |
 _____
```
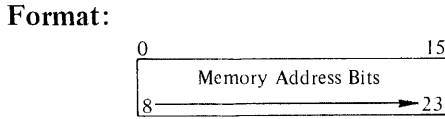
Function:
Causes the channel to place the contents of its
task register on the bus.

Command:
   Input Memory Byte Address

Function Code:
   08

Format:

```
0                               15
 ┌─────────────────────────────┐
 │   Memory Address Bits        │
 │ 8───────────────────────►23  │
 └─────────────────────────────┘
```
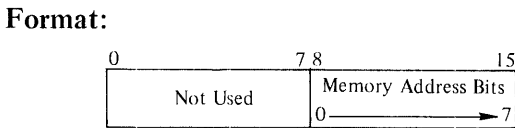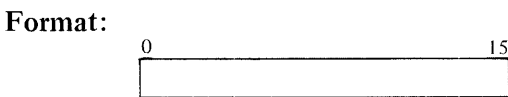
Function:
   Causes the channel to place the 16 least significant bits of its DMA address register on the data bus. The bits represent the memory address register bits 8-23.

   Note: This command will violate memory protection.

Command:
   Input Memory Module Address

Function Code:
   0A

Format:

```
0               7 8             15
 ┌─────────────┬───────────────┐
 │             │ Memory Address Bits │
 │  Not Used   │ 0──────────►7 │
 └─────────────┴───────────────┘
```

Function:
   Causes the channel to place the eight most significant bits of its DMA address register on the data bus. The bits represent memory address bits from 0 through 7 inclusive.

   NOTE: This command will violate memory protection.

Command:
   Input Range

Function Code:
   0C

Format:

```
0                               15
 ┌─────────────────────────────┐
 │                             │
 └─────────────────────────────┘
```

Function:
   Causes the channel to place the contents of its range register on the data bus.

Command:
   Input Status Word 1

Function Code:
   18

Format:

```
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15   Status Word 1
```
- End of Form
- Attention
- Device Ready
- Non Correctable Memory Error
- Bus Parity
- Non-Existant Resource
- Corrected Memory Error
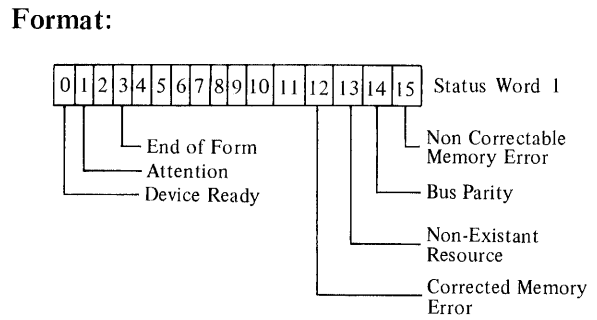
Function:
   Causes the channel to place the contents of its first status register on the bus. See also Table 6-18.

Command:
   Input Status Word 2

Function Code:
   1A

Format:

```
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15   Status Word 2
```
- End of Form
- Attention
- Device Ready
- Non Correctable Memory Error
- Bus Parity
- Non-Existant Resource
- Corrected Memory Error
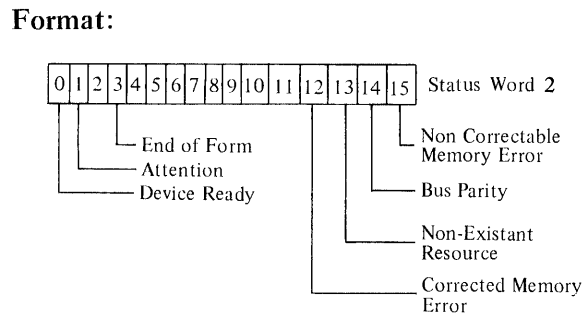
Function:
   Causes the channel to place the contents of its second status register on the bus. See also Table 6-18.

   Errors during data transfer will be indicated by a status erport at the end of the record.

   Errors on I/O Commands from the CP will set the appropriate status bit and immediately interrupt the CP. The I/O Command will be acknowledged normally and stored in the MDC memory but will not cause any further action. If interrupts are blocked (Level = 0), the command in error will be used as if there were no error.

Command:
   Input Device ID

Function Code:
   26

Format:

```
0                               15
 ┌─────────────────────────────┐
 │                             │
 └─────────────────────────────┘
```
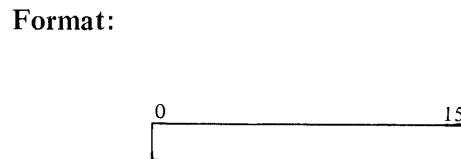
TABLE 6-18. STATUS BIT DEFINITIONS – SERIAL AND LINE PRINTERS

Status Condition	Bit	Definition	Reset By
Device Ready	0	Printer power on. No faults. Paper loaded. No open interlocks. Switches in correct positions.	A change in conditions.
Attention	1	The device ready condition has changed.	Reading Status word 1 clears this bit.
End of Form	3	The printer has detected End of Form either by VFU, if equipped, or otherwise by precon-figured line count.	Next IOLD Command.
Corrected Memory Error	12	The memory read response was accompanied by a signal indicating the error was corrected.	Next IOLD Command.
Non-Existent Resource	13	A NAK was received from memory. Indicates possible programming error (non-existent memory).	Next IOLD Command.
Parity	14	The parity was incorrect on a bus transfer toward the MDC.	Next IOLD Command.
Uncorrectable Memory	15	The memory read response was accompanied by a signal indicating an error existed that could not be corrected.	Next IOLD Command

Function:

Causes the channel to place its device identification number on the data bus.

- Serial Printers — 2004 (PRU9101)
  2006 (PRU9102)
- Line Printers — 2000 (PRU9104/9106)
  2001 (same as above but with PRF9102)
  2002 (PRU9103/9105)
  2003 (same as above but with PRF9102)

Specifications

Paper Stock: Width — 4.4 in. (11.4 cm) to 14.8 in. (37,8 cm). Weight — Standard fan-folded and edge-punched: 15 lb. (6,82 kg) minimum; multicopy: 12 lb.(5,45 kg) maximum; with carbon: 6 lb. (2,73 kg) for 5 parts.
Programmed Operations: Print only; space only, space and print.
Device Interface: Each serial printer requires its own Printer Device-Pac (PRM9101).
Printable Characters: PRU9101 — 64-character set: 10 numeric, 26 alphabetic, and 28 special symbols;
PRU9102 — 96-character set: 10 numeric, 52 alphabetic, and 34 special symbols.
Print Format: 132 print positions per line, 10 characters per inch. Vertical spacing is 6 lines per inch.

Print Speed: 60 lines per minute at 132 characters per line.
Matrix Font: 9 x 7 Dot; equivalent to 10 point type.
Physical Characteristics: Height — 11.10 in. (29,2 cm);
Width — 2.4 ft (70,4 cm); Depth — 1.6 ft (50,7 cm);
Weight — 118.3 lb. (53.6 kg).
Required Input Power: 120 Vac + 10%, -15%; 60 Hz ± 1/2 Hz, 450V Amps.

LINE PRINTERS

The Types PRU9103/9104/9105/9106 Printers are designed to provide 6/30 Model users with high-quality printed output at medium to high print rates of 240 to 600 lines per minute (lpm) (Figure 6-20). The PRU9104/9106 and PRU9103/9105 have 64- and 96-ASCII character code sets, respectively. All printers offer 136-column printing and provide for vertical spacing of six or eight lines per inch. Format flexibility can be greatly enhanced via Option PRF9102 Vertical Format Unit which enables paper spacing to be controlled by a 12-channel paper tape. The flexibility of upper and lower case printing is available with the PRU9103 and 9105.

The printers interface with the Level 6 processor by means of a single-board Multiple Device Controller (MDC9101), a Printer Device-Pac (PRM9101) and a 50-foot (max length) cable.
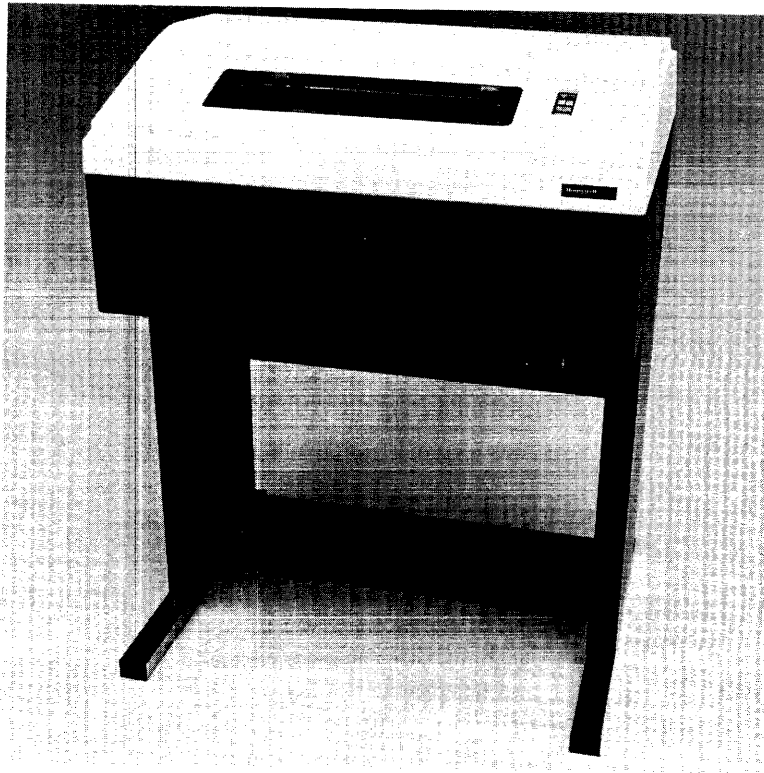
Figure 6-20. PRU9103/9104/9105/9106 Printers

Features
- Original and up to five copies
- Simplified operation — fault indicator panel included for rapid identification of operator-correctable problems
- Easy paper loading with front-access, swing-open, drum gate mechanism
- Full line (136 characters) buffer, loaded at 5-10 μs per character under DMA control
- Byte-mode addressing conserves memory
- Six/eight-lines per inch selection
- Separate offline test mode for easy maintenance
- Upper/lower print capability with PRU 9103/9105

Operation
Printing operations for printers without the VFU option include:

- Print without spacing
- Space one to fifteen lines
- Space one to fifteen lines and print
- Space to head of form and print

For printers with the VFU option the following operations can also be performed:

- Space to channel 1 (or channels 2 through 12) and print

- Space to channel 1 (or channels 2 through 12) and do not print

All data transfers are under DMA (Direct Memory Access) control. While the printer is busy, the computer is free to perform other operations.

Instructions
The instructions and programming information presented for the serial printers is also applicable for the line printers.

Specifications
Print Speed: PRU9103 — 240 lpm; PRU-9104 — 300 lpm; PRU9105 — 480 lpm; PRU9106 — 600 lpm.
Columns Per Line: 136
Line Advance Speed (one line): 50 ms (max)
Paper Slew Speed: 20 ips (min)
Vertical Spacing: 6 or 8 lines per inch
Printable Characters: PRU9103/PRU9105 — 96-character set, upper and lower case ASCII code; PRU9104/PRU9106 — 64-character standard ASCII code set.
Paper Stock: Standard fan-folded and edge-punched: 4.01 inches (10.2 cm) to 15.98 inches (40.6 cm) wide, with 11.02 inches (28.0 cm) between folds. When VFU option is present, distance between paper

folds may be varied from 4.01 inches (10,2 cm) to 17.99 inches (45.7 cm) at 8 lines per inch, or 4.01 inches (10.2 cm) to 23.97 inches (60.9 cm) at 6 lines per inch. Weight — For single copy: 14.93 pound (6.72 kg) bond (min) For up to six copies: 12.22 pound (5.5 kg) bond with carbon (min). Maximum form thickness — 0.023 inches (0.0508 mm)

Device Interface: Each printer requires its own Device-Pac (PRM9101)
Physical Dimensions: Height — 45 in. (114 cm) high:
Width — 33 in. (81.3 cm) wide; Depth — 22 in. (56 cm)
Weight: 340 lb (150 kg)
Required Input Power: 115/220 Vac ± 10 %, 50 or 60 Hz ± 2 Hz, single phase, 525W

SECTION 7

SOFTWARE

Level 6 offers both a basic and an extended software capability in packages called, respectively, GCOS/BES1 and GCOS/BES2.

GCOS/BES1

GCOS/BES1 performs the chief system functions, allowing you to concentrate on your applications. Figure 7-1 provides an overview of the various modules, languages, programs, and development tools.

Program Development Tools

The program development tools operate in an offline environment and are comprised of: a Command Processor that interacts with the Loader to bring the other system modules into memory, two language processors — a FORTRAN Compiler and an Assembler for the Level 6 Assembly Language, an Editor for correcting the source text of programs written in either language, a Linker that converts object modules from the Assembler or the compiler into an executable form, and a Cross-Reference Program, which is a utility that relates the symbolic tags of an assembly program to the listing line numbers where they appear. Figure 7-2 summarizes the sequence of events that might take place during the development of an application program.

Command Processor

The Command Processor loads all system and application programs via console commands that initiate the following functions:

- Places information in the Loader communication block.
- Builds an Attach Table.
- Builds an Argument List.
- Sets addresses in the appropriate registers for the argument list and the program's return address.

GCOS/BES1 SOFTWARE

EXECUTIVE MODULES
- TASK MANAGER
- CLOCK MANAGER
- OPERATOR INTERFACE MANAGER
- BUFFER MANAGER

UTILITY PROGRAMS
- UTILITY SET 1
  INITIALIZE VOLUME/FILE, ALLOCATE, DELETE, LIST, DUMP, REPLACE, RENAME
- UTILITY SET 2
  PRINT, DUMP LOGICAL FILE, DUMP PHYSICAL DISKETTE, DISKETTE TO PAPER TAPE, CARD/PAPER TAPE TO DISKETTE
- UTILITY SET 3
  COPY, COMPARE
- DEBUGGER
- PROGRAM PATCH

PROGRAM DEVELOPMENT TOOLS
- COMMAND PROCESSOR
- EDITOR
- ASSEMBLER
- FORTRAN COMPILER
- LINKER
- CROSS-REFERENCE PROGRAM

PROGRAMMING LANGUAGES
- ASSEMBLY LANGUAGE
- FORTRAN (ANSI 1976)

INPUT/OUTPUT MODULES
- ONLINE ELEMENTS
  - FILE MANAGER
  - FORTRAN RUN-TIME I/O ROUTINES (FRIOR)
  - DRIVERS
    CARD READER
    PRINTER(S)
    CONSOLE (KSR/ASR)
    DISKETTE

OTHER SOFTWARE
- CONFIGURATION LOAD MANAGER
- LOADERS
  DISKETTE
  PAPER TAPE
- FORTRAN MATH ROUTINES
- FLOATING-POINT SIMULATOR
- TRACE TRAP HANDLER

Figure 7-1. Software Overview
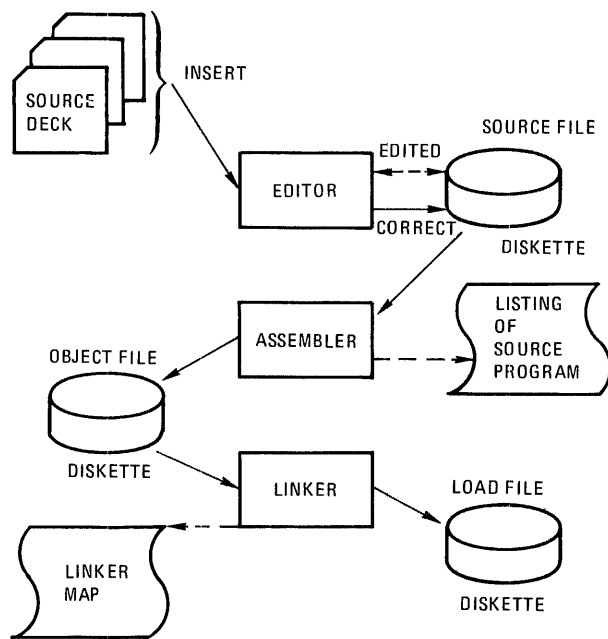
Figure 7-2. Program Development Sequence

The Command Processor responds to these console commands by providing the Loader with the precise directions necessary to load the requested system or application program. The four commands are:

- Load Initialize — specifies a relocation factor for the program being loaded and provides a post-load option of either halt or execute.
- Attach — provides the name, logical file number, symbolic device name, and channel number for each file used by the program to be loaded. One Attach command is necessary for each file, including the one the program to be loaded resides in. The Command Processor uses the information from this statement to build the Attach Table.
- Detach — deletes entries from the Attach Table, initializes all except the standard system entries, and "repacks" the table by altering the table displacement in the first word of the Attach Table.
- Load — provides the member name of the load module to be loaded and whatever arguments are needed by the module. The Command Processor uses the information from this command to build the Argument List and sets a bit in the Loader indicator word of the Loader communication block to indicate that there are arguments to be passed.

The Command Processor also places the address of the control word of the Argument List into register B7 and sets a value in register B5 for the return address.

Editor

The Editor is a system program that enables you to correct the source text of application programs written in either the Level 6 Assembly Language or FORTRAN. Editor accepts its source file input from diskette and writes the corrected source program out to diskette. The command file that directs Editor's operation can come from a KSR, paper tape on an ASR, or a card reader.

If the source program to be corrected is not already on diskette, the file can be created by using the INSERT command, followed by the text for the file and the appropriate commands to terminate the insert and close the file. The Program Development Tools manual details all the Editor commands for locating, substituting, deleting, and inserting statements in source programs.

Once you have written and edited your application program, it must be assembled or compiled using one of the system programs.

Assembler

The Level 6 Assembler is a system program that processes Assembly Language source code, translates these statements into object code acceptable to the Linker, and produces a listing of the source statements and their associated machine code equivalents, suitably flagged for error conditions.

The Assembler is a two-pass program that runs in a minimum configuration of 8 KW. The first pass generates the symbol table in the Assembler's resident table area; the second pass generates the object module and a listing if requested.

The Assembler accepts the input commands that control its operation from a KSR; it accepts source statement input from disk. The Assembler output, both the object module and the list, can be written to diskette, as well as assigned directly to a printer.

FORTRAN Compiler

The FORTRAN Compiler translates source statements written in that language into either an object module ready for processing by the Linker or a file of assembly language instructions for further processing by the Level 6 Assembler. The compiler is a single-pass processor that operates in 16 KW of memory.

The compiler is invoked by a command entered through the console; it accepts its source input from diskette and produces its object module or assembly language source module on diskette. The Compiler also produces a listing of the source text with imbedded diagnostics and a memory map that is directed either to a diskette (for printing later) or to a printer.

Two sets of routines are available for use with FORTRAN programs: basic external functions and intrinsic functions. The basic external functions are frequently used mathematical routines; the intrinsic functions are a set of fundamental operations that are difficult to express in FORTRAN statements and, hence, are written in Assembly Language for use with FORTRAN programs.

Linker

The Linker converts object modules that are the output of the compiler or the Assembler to a format acceptable to the diskette loader. It resolves external references and can process one or more object modules to produce a single load module or several load modules in one execution.

The Linker is controlled by command statements that are entered through a console. The Linker input and output files must be on diskette. Linker also produces listings containing a link map and error messages that can be output to a console printer, line printer, or spooled to diskette for later printing.

Cross Reference Program

A Cross Reference Program, provided for use with Assembly Language source programs, reads the source statements and produces an alphabetized listing of cross references (i.e., symbol definitions and where they are used) for the program. This Cross Reference Program keeps a tally of the number of times each symbolic tag is used, and which statements the symbol occurs in so that when a problem arises, all corrections to a particular entity can be made at one time.

Utility Programs

The system programs designated as utilities provide a variety of services for volume preparation and maintenance, file handling, and data transfer from one type of medium to another, as well as program debugging and patching of either object or load modules on diskette files. These utility programs only execute in the offline environment and require the Command Processor. The following descriptions are very brief, for complete details see the GCOS/BES Utility Programs manual.

Utility Set 1

Utility Set 1 performs diskette volume and file preparation and maintenance. One of its functions is to initialize new diskette volumes for use with the diskette drive and to allow the volume to be processed by the system file handling routines. Initialization consists of writing the bootstrap record, the loader, and volume directory information on track zero of cylinder zero of the volume.

Other functions are:

- Allocating space for new files.
- Deleting files or members.
- Initializing partitioned files.
- Listing contents of volume directories and member names of partitioned files.
- Dumping information from a diskette to a memory area or from memory to diskette or to a console, line, or serial printer.
- Replacing one memory value with another.
- Renaming a volume or a file.

Utility Set 2

Utility Set 2 provides the following data transfer functions:

- Printing a file or member.
- Dumping a logical file or member.
- Dumping a physical diskette.
- Transferring file or member from diskette to paper tape.
- Transferring card or paper tape file to diskette.

Utility Set 3

Utility Set 3 provides for copying and verifying diskette data, including:

- Copying a volume, file, or member from one diskette to another.
- Comparing the new volume or file (but not a partitioned file or member) with the original to verify the accuracy of the copy operation.

Debugger

Debugger is an interactive utility used for program testing and error correction. The console dialogue consists of commands submitted by the operator and responses displayed on the console printer in the form of informational and error messages. Debugger can display and modify memory addresses and register contents. The "breakpoint" feature of the utility causes the automatic activation of Debugger when a specified operation code occurs in the program being executed. When the utility terminates, it automatically transfers control back to the executing program.

Program Patch

The Program Patch utility allows the alteration of either object or load module text. Patches can be created, added, deleted, and listed by using the appropriate commands to the utility.

Executive Modules

The Executive software is a basic set of support facilities enabling you to develop your application programs around such system-supplied features as clock-initiated tasks, automatic task scheduling and dispatching based on a flexible priority/ interrupt structure, and the trapping of certain conditions arising out of program execution, without adding to your software overhead. Figure 7-3 shows the interrelationships of the Executive modules.
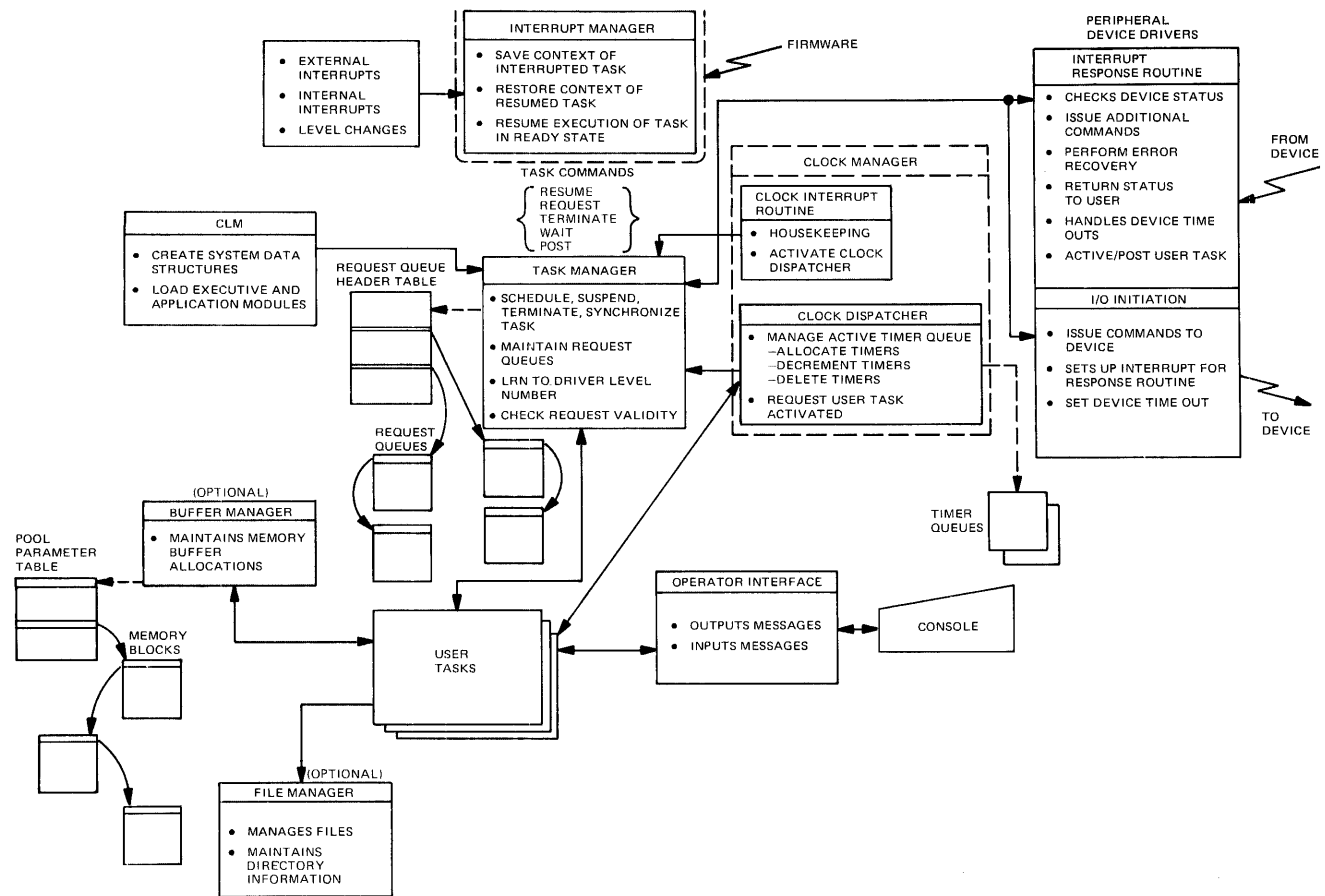
Figure 7-3. Interrelationships of the Executive Modules

Task Manager

This Executive component, supported by firmware and hardware functions, schedules, dispatches and synchronizes tasks. To maintain the various task states shown in Figure 7-4, a number of data structures are defined when the online environment is configured. These structures are:

- Priority level activity indicators
- Interrupt vectors
- Interrupt save area (ISA)
- Request queues

Priority Level Activity Indicators

Each of the 64 priority levels is associated with an activity indicator bit in a 4-word contiguous area in a dedicated main memory location. Each bit in the 4-word area indicates whether or not its respective priority level is active. Bit zero of the first word indicates activity of a priority level zero task when this bit is on (equal to one); bit 15 of the fourth word indicates activity of a priority level 63 (system idle) task. When the level is inactive, its respective bit is equal to zero.

Interrupt Vectors

Interrupt vectors are pointers to priority level specific entries in the interrupt save area (ISA). Each vector is one word long and contains either zeros if no task is using that particular priority level, or the address of the location of the ISA related to that task's level. There is one vector for each of the 64 priority levels and the 64-word area is in a dedicated main memory location.
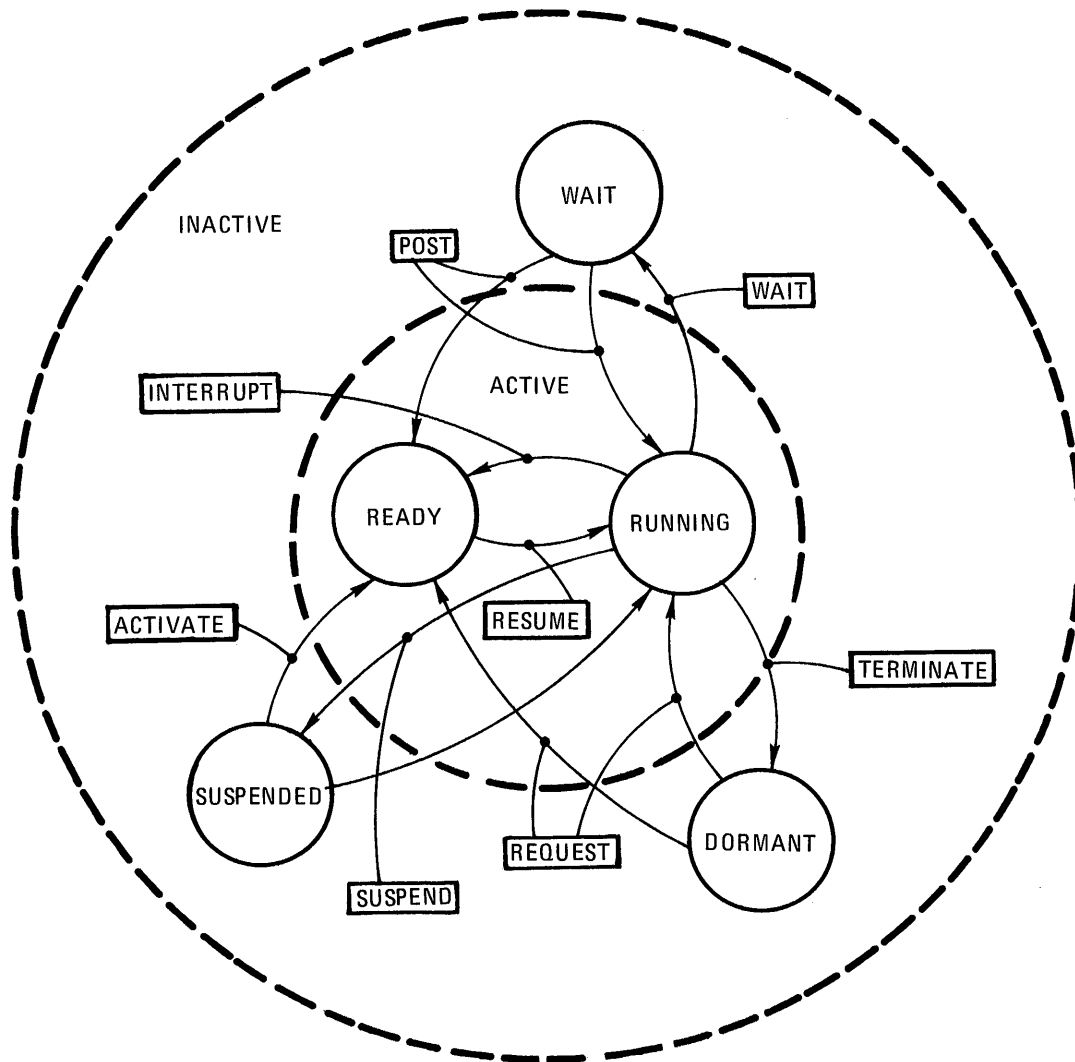
Figure 7-4. Task States

Interrupt Save Area

This structure, residing in a nondedicated area of main memory, is where the context of an interrupted task is saved, and from which that context is restored when the task is restarted. A task's context consists of its registers and several other necessary pieces of information for restarting the task. You can select the number of registers that are saved/restored. There is one ISA for each priority level in use except for level 3, the inhibit level. (See Figure 7-5.)

Request Queues

These structures coordinate requests for the execution of tasks. The request queues, one for each priority level, consist of header tables and request blocks threaded together in a forward direction. (See Figure 7-5.)

The request queue header tables contain pointers to the request blocks for each priority level. The start-of-queue (SOQ) header table contains pointers to the first request block associated with each priority level. Each request block in turn points to successive request blocks for that level's task, until a block is reached that contains zero in the "next entry" pointer, indicating that the last block in the queue has been reached. The end-of-queue (EOQ) header table points directly to the last block in the queue.

The request blocks themselves are variable length areas of contiguous main memory. They contain information for task management such as the task's level and status, and any other data in the form of temporary storage or values needed by the task.

Management of Task States

The task states shown in Figure 7-4 are managed by interactions of software routines with hardware and firmware functions. The hardware in task management saves and restores task contexts.

Firmware functions that alter task states are:

● Activate — mark the level as active (followed by Resume).
● Suspend — mark the current level as inactive (followed by Resume).
● Resume — examine the level activity indicators for the highest active one and start task.
● Inhibit — mark a dedicated, high priority level as active and immediately start a task on this level. The running task continues on this level with no context save or restore.
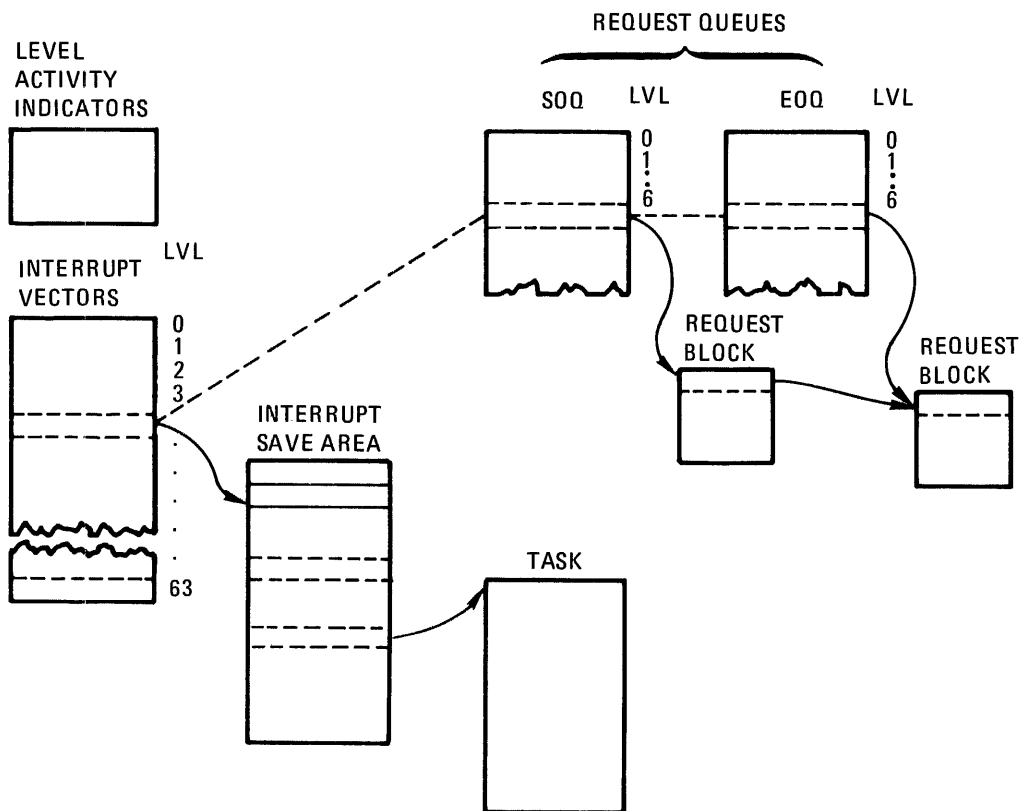
Figure 7-5. Task Management Data Structures

- Enable — return a task to its normal level from the inhibit level.

The software functions that alter task states are:

- Request — supports the capability to request the activation of a task.
- Wait — provides for a running task to be put in the wait state to allow the completion of another task that was called by the running task.
- Post — provides for the reactivation of a waiting task, and the termination of the task being waited for.
- Terminate — ends a running task and unlinks the associated request block.

Clock Manager
This Executive component controls the connecting, disconnecting, and processing of the clock timer blocks and the system control structures used for the timing of tasks by the Executive software.

The clock timer blocks are defined by the user according to application requirements and then are maintained by the Clock Manager and used to activate tasks at given priority levels after an elapsed time interval or at some regular time interval.

The Clock Manager subroutines provide the following services:

- Connect the clock timer blocks.
- Disconnect the clock timer blocks.
- Convert the time of day to ASCII format.
- Convert a millisecond value to a clock-compatible value.
- Convert the date to ASCII format.

Each subroutine provides a return status indication when it finishes execution.

Operator Interface Manager
The Operator Interface Manager controls all operator dialogue with software in an online environment. It presupposes a keyboard-send-receive (KSR) device that not only prints out messages to the operator, but also accepts information from a keyboard.

The component uses three kinds of messages:

- Information message — consists of an automatic line feed, message text, and automatic carriage return.
- Prompter message — solicits an operator response, and consists of a line feed, text and question mark.
- Reply message — enables an operator response to a request for information or other specific input.

Buffer Manager
This Executive component manages the system and user-requested memory space. The memory space used for buffer areas is defined when the online environment is configured. (See also "Configuration Load Manager.")

When the Buffer Manager receives a request for buffer space, it searches the predefined control structures and related buffer pools for the appropriate space. Even if a request is made for a block size that is not specifically defined, the request can be filled with a block of the next larger defined size.

When a block of the appropriate size is found, the Buffer Manager then supplies the requesting program with the address of the block along with a return status indicating a normal operation. If the request cannot be honored, the returned status indicates either invalid size, if the requested buffer was larger than the largest defined buffer block, or it indicates that the pool of the requested size is empty, that is, no blocks are available.

After a program has finished using a buffer area, it can indicate that it no longer needs the space, and the Buffer Manager reconnects the area to the pool, thus making it available for use again.

Input/Output Modules
The software components that provide data input and output services consist of several groups of modules; some are provided for online environments exclusively, others execute in an offline environment.

The modules that provide online input and output services are a File Manager, a set of FORTRAN Run-Time Input/Output Routines (FRIOR), and a set of device drivers. The offline input/output services are provided by a set of device drivers.

File Manager
The File Manager consists of a set of service routines that provide access to volumes and files in an online environment. Among the routines provided by the File Manager are those to open, read, write, and close files, as well as routines to supply file status information, to position files. The File Manager also returns error information for the various functions it performs.

FORTRAN Run-Time I/O Routines (FRIOR)

These routines provide for data transfer, device implementation, and the processing of FORTRAN format statements; since these routines require the services of the File Manager, they are used only with programs that are executed in an online environment. These routines provide for the reading and writing of formatted and unformatted records and they contain data conversion routines to edit integer, real, logical, character, and Hollerith data for formatted input and output. The FRIOR produce diagnostic messages to inform the user of inappropriate or inconsistent commands.

Device Drivers

These device-specific software components perform all data transfers between system and application programs and their respective devices. There are drivers for all Honeywell-supplied input and output devices operating in online environments.

The drivers are linked with the Executive modules and receive requests for service from the Task Manager. Online device drivers run at the priority level of the requested device.

Line and Serial Printer Driver

This component drives both line and serial printers. Its functions are:

- Initiating output on individual printers.
- Reporting errors and status information.
- Timing to detect a device failure.
- Replacing tab characters with spaces.

Card Reader Driver

This component drives card readers. Its functions are:

- Initiating input on individual devices.
- Suspending itself to wait for interrupt from device.
- Checking device status.
- Timing to detect a device failure.
- Reporting device errors and status.

Diskette Drivers

This component manages data transfers to and from diskettes. The driver is interrupt driven and requires the Task Manager. The driver must be permanently resident; it does not verify the volume identification so you must ensure the correct volume is mounted. Diskette driver functions perform the following:

- Manage all standard data transfers.
- Provide callable functions for reading and writing data.

The driver performs neither diagnostic read/write nor write-deleted-data functions; all formatting must be done offline, using the utilities.

Console (KSR/ASR) Drivers

Teletype device drivers that manage data transfer exist as separate, device-specific modules. You link the particular module(s) for the device to be used.

The driver for the KSR device provides keyboard and printer functions. The driver for the automatic-send-receive (ASR) device consists of the KSR driver linked to modules that provide paper tape read and punch functions.

The online drivers (KSR and ASR) respond to requests from the Task Manager and run at the priority level assigned to the device.

Briefly, the functions of the teletype drivers are to:

- Initiate I/O on individual functional units.
- Report errors and status information.
- Detect device failure/inactivity during input.
- Report use of Break key to operator interface or user-supplied routine (online).

In addition, the ASR drivers provide these functions:

- "Escape" special control characters for paper tape.
- Perform checksum calculation and verification for paper tape.
- Provide format and format checking for paper tape.
- Support paper tape punch in automatic mode.

Other Software

Configuration Load Manager

This component builds and initializes the online system and starts execution. The Configuration Load Manager (CLM) uses information supplied to it to define system characteristics and build some of the data structures that the Executive software uses to control the processing of tasks.

CLM accepts commands that set up data structures for the Task Manager, devices, trap handling, as well as the clock variables and a list of load modules to be included in the complete

system. The CLM performs in two phases: the configuration phase and the loading phase. During configuration, CLM creates the system data structures and stores them in main memory; the load list is created for use in the next phase.

During the loading phase, the various Executive and application modules are brought into memory. Each module contains permanently resident code and some temporary code for initialization of the module. The temporary code is overlaid by the permanent code of the next loaded module.

During this phase, defined symbols are added to the symbol table and references are resolved. Once a load module is in memory, control is transferred to its initialization code; whatever initialization is required by the module is performed. Control is then given back to the Loader to begin loading of the next module. This process continues until all modules are loaded, at which time, control is given to the highest priority Executive module and execution begins. See Figure 7-6 for memory layouts during the two phases.

Loaders

Loaders are device-specific software components that load executable modules into memory from their respective devices and turn control over to the module. Loaders are available for bringing modules into memory from diskette as well as paper tape.

Diskette Loader

The Diskette Loader resides on the system load module diskette. It is brought into memory by a firmware bootstrap routine that causes the loader to read into memory and turns control over to the loader itself. The Diskette Loader includes four routines: loader initialization, Command Processor calling sequence, main loader, and miniloader.

At the entry point of the loader initialization routine, control is returned to the loader by the bootstrap routine. When the loader initialization routine finishes processing, the area it has occupied becomes available for use as the loader buffer area. The functions of the loader initialization routine are to:

- Save the bootstrap address for the miniloader.
- Store the HALT address in the loader communication area.
- Set values for the diskette loader and the processor type in the loader indicator word.
- Load the trap handling routine that initializes the hardware dedicated locations.
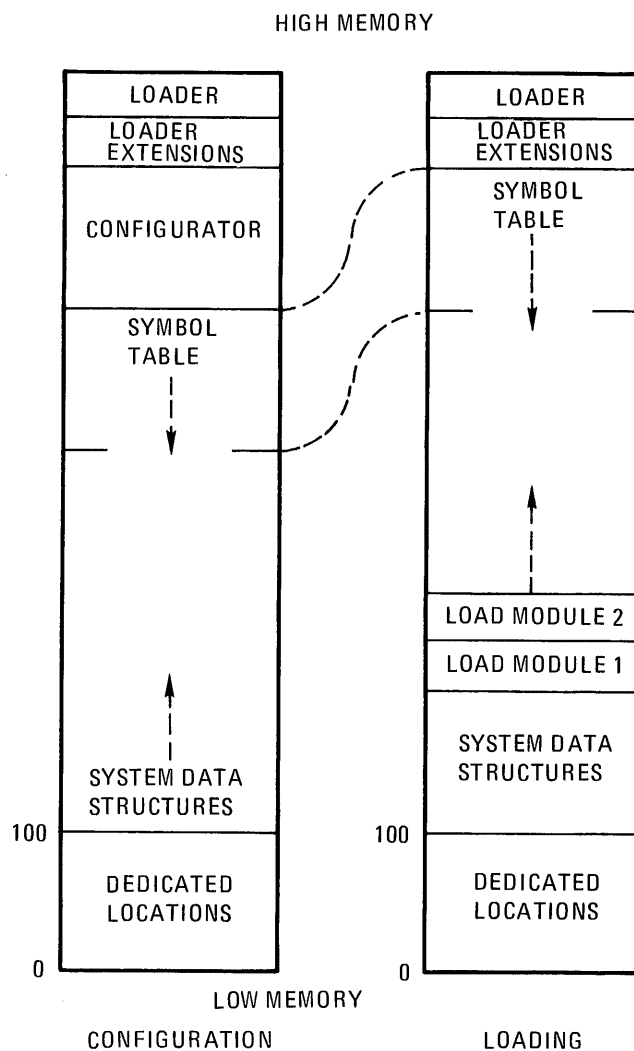
Figure 7-6. Memory Layouts During Operation of CLM

- Transfer control to the Command Processor calling sequence.

The Command Processor calling sequence primes the load parameters in the loader communication area to load the Command Processor. Its functions are to:

- Initialize the relocation factor to zero.
- Initialize the program loading channel to the bootstrap channel.
- Set the file and member names for the Command Processor.
- Transfer control to the main loader.

The main loader routine searches for and loads the requested member. It reads the member, a sector at a time; analyzes the item type of the sector; and relocates and distributes the code. The main loader also resolves backpatch chains and

relocates global addresses depending on the item type. When the loader finishes processing, it turns control over to the designated entry point of the loaded module.

The miniloader routine, which at some times during processing may be the only resident part of the loader, is the basis of the software bootstrap routine. The miniloader contains:

- A basic diskette I/O routine.
- Loader communication area (displacement of loader entry points, Attach Table reference point from high memory, loader parameters, and halt addresses).

The miniloader reloads the boot loader at the bootstrap address, which in turn loads the diskette loader.

Paper Tape Loader

The paper tape loader resides on paper tape and is brought into memory by a firmware bootstrap routine that causes the loader to be read into memory and turns control over to the loader itself. The paper tape loader consists of two routines: the loader initialization routine and the main loader.

The loader initialization routine is entered from the bootstrap routine. After it has executed, the area the initialization routine has occupied is available as a buffer area for the main loader. The loader initialization routine has these functions:

- Save the bootstrap channel number.
- Store the halt address for conditions requiring operator intervention.
- Load the trap handler module that initializes the dedicated hardware locations.
- Branch to the entry point of the main loader when all functions are complete.

The main loader routine loads the requested load module from paper tape into memory. The main loader read the load text, a block at a time; analyzes the item type; distributes the code; relocates addresses; and resolves backpatch chains. When the loading is completed, the main loader turns control over to the loaded program.

FORTRAN Mathematical Routines

Level 6 software includes a large set of FORTRAN mathematical routines. These intrinsic functions are available in object module format so they can be linked on an as-needed basis to perform a variety of calculations on behalf of a FORTRAN program. Some of the calculations performed by these routines are:

- Converting to and from integer and real values.
- Truncating.
- Determining nearest whole number.
- Transferring a sign.
- Choosing the largest value, the smallest value.
- Finding the length of an entity, the square root, the natural logarithm, the common logarithm.
- Computing selected plane and spherical trigonometric functions.

See the GCOS/BES FORTRAN manual for details about these routines.

Trap Handling

A trap is a conditional jump made to a predefined location in response to some event that occurs during program execution. Unlike interrupts, which are responses to events that are either unrelated to, or at least asynchronous with, the currently executing program, trap conditions are caused by the executing program. Series 60 (Level 6) hardware can be enabled to recognize and trap sixteen different conditions arising during program execution. The enabling is done by a trap handler module that is invoked by the initialization routines of either the diskette or paper tape loaders.

The trap handler sets up trap vectors in dedicated locations in main memory, provides trap save areas, and interrupt save areas.

Level 6 software supports two trap handling facilities. These are the trace trap handler and the FORTRAN floating point simulator. All other occurrences that result in a trap cause a halt in processing.

Trace Trap Handler

Briefly, the trace trap handler maintains a history of specific system parameters such as the program counter (P-register), the system status register (S-register), memory location contents, data and address registers, depending upon the contents of the register save mask, for each "break trap" instruction used in the program.

FORTRAN Floating-Point Simulator

The FORTRAN floating-point simulator allows the simulation of scientific instructions on machines that do not have the scientific option installed. (See Executive and Input/Output manual for trap handling details.) Users of the floating-point simulator who wish to use the hardware floating point in the future should recompile their programs under FORTRAN.

GCOS/BES2

GCOS/BES2 includes all the capabilities of GCOS/BES1 with significant extensions in communications, executive functions, and program development tools. Among the new communications capabilities are support of a BSC link to a host computer and an operator interface. Added executive functions include a disk-based system for loading/activating tasks resident on either diskette or cartridge disk. And the program development enhancements encompass extensions for both the Assembler and the FORTRAN Compiler and a macro preprocessor. There are still other capabilities in such areas as file management, utilities, job stream management and teleprinter/console display support.

Program Development Job Stream

The program development system can operate in either an interactive (single user) or a batch mode. Batch mode operation is a new feature added to BES2 that allows program development jobs to be predefined and stored in a file on cartridge disk, diskette, or cards. Then the Command Processor executes the job by reading that file, thus eliminating operator intervention except where it is desired, or required, to mount volumes, etc.

Macro Preprocessor

The macro preprocessor is an offline program development component that operates in 8 KW of memory. It scans an assembly language source program for macro calls. Each macro call and its parameters are analyzed and replaced by assembly language source statements that are retrieved either from a definition in that source program or from a library file. The macro calls and their expansion definitions (macro prototypes) are defined by the programmer. There can be up to 35 parameters described for a macro call. Local and global macro variables are supported. In addition, you can nest macro calls within a macro prototype.

FORTRAN Enhancements

The FORTRAN Compiler provides a number of significant enhancements; most are related to FORTRAN ISA extensions for process control applications. For example, the ISA executive interface (CALL, START, TRNON, WAIT), ISA bit string manipulation (IOR, IAND, IEOR, NOT, ISHFT, IBTEST, IBSET, IBCLR), and the ISA date and time functions are now available.

Executive

A number of enhancements in the online execution area are included, specifically, tasks can now be disk-resident and initiated by either another task or a message from the console. The operator's console can be attached through an MLCP. The task management capability is also extended with such features as simultaneous multitasking per priority level and more complex WAIT functionality.

Communications

Communications is supported at two different levels. At the logical I/O level, a programmer can treat a communications terminal as if it were a file (e.g., using OPEN, CLOSE, READ, WRITE). At the physical I/O level, more detailed control of the terminal and line is available. Teletype Model 33 and 35 terminals are supported, along with Teletype-compatible CRTs. BSC (2780) is also supported (ASCII nontransparent and EBCDIC transparent modes).

SECTION 8

SITE PREPARATION PLANNING

INTRODUCTION

This section provides Level 6 users with an overview site preparation planning that will help ensure a successful minicomputer installation. Requirements vary from user to user, depending on the way the Level 6 equipment is to be utilized. Users with specialized configurations (e.g., message concentration or remote batch processing) or incorporating selected Level 6 components into their own configured systems will find the planning arrangement of this section useful.

So as to be useful to the maximum number of Level 6 users, this section has been made as comprehensive as possible. All Level 6 users should discuss site preparation with their Honeywell Marketing Representative, to determine the type and amount of installation assistance that would be of the most benefit to them.

Site preparation requirements begin with the configuration, followed by the layout, specifications and facilities (see Appendix A) of a system and minicomputer room.

Honeywell Marketing Representative or Field Engineering must be consulted if any characteristics of the site do not meet the requirements specified in this manual or to answer questions concerning content of this section. In some cases, unit and system requirements are subject to change, both in modification and design, as engineering improvements are implemented. This information will be distributed to you as it becomes available.

Table 1-1 outlines the sequence of events in site preparation and planning. It describes the steps to be taken and the assistance Honeywell provides in carrying out the installation of a Level 6 system. The same emphasis that is given to programming and system design should be placed on selective site preparation and installation procedures. In some cases, (during site preparation) when a schedule changes, the sequence of events may vary.

TABLE 8-1 INSTALLATION CONTRACTED RESPONSIBILITIES

What You Do	What Honeywell Does to Help You Under Contract
Select site for your system	Decides upon space for your system to best utilize a recommended layout.
Prepare site	Furnishes complete air conditioning and electrical specifications for system and associated peripherals.
Determine the time of shipment Alert Marketing Representative if delivery difficulties are anticipated, i.e., second floor delivery, small elevator, no receiving dock, etc. Accept Delivery	Honeywell carefully packs equipment for shipment to you by best shipping method to suit your particular requirements. Movers place all equipment in position according to your layout. Installs and connects all Honeywell interconnecting cables and, where applicable, connects the ac plugs. The system is thoroughly checked out and turned over to you.

NOTE: All equipment that is not manufactured or supplied by Honeywell is customer's responsibility unless subcontracted to Honeywell in writing.

CONFIGURATION

The actual configuration of a Level 6 system depends on the users present requirements and expansion needs. Honeywell has built expansion capabilities into the Level 6 to provide for increased customer workloads without the need for additional mainframes.

After you have established your overall system requirements you must select the compatible central processor modules, general options, semiconductor, RAM memories, and memory save, components and accessories, peripherals, expansion cabinets and power distribution units to meet your needs. Level 6 systems can be figured manually using the information in this document.

A summary of features and options for Models 6/34, 6/36 (5 slot Megabus Chassis) and 6/36 (10 slot Megabus Chassis) is given in Table 8-2.

TABLE 8-2. CENTRAL PROCESSOR SUMMARY

Description	Model 6/34 CPS 9450	Model 6/36 CPS 9460	Model 6/36 CPS 9461
Central Processor • Megabus Chassis with Power Supply • Multiply/Divide Hardware Real Time Clock • ROM Bootstrap Loader for Keyboard Console, Diskette and Card Reader	Included	Included	Included
Model 6/34 Processor in 4 slot Megabus Chassis with basic control panel, memory controller with parity and an 8K word Memory-Pac.	Included	Included	—
Three additional type CMM9001 8K Memory Pacs can be added for a total of 32K maximum.	Optional	—	—
Model 6/36 Processor in 5 slot Megabus Chassis with full control panel.	—	Included	—
Memory controller with 8K-word Memory-Pacs, Types CMC9001 and CMC9002 for up to 64K.	—	Required	—
Model 6/36 Processor in 10 slot Megabus Chassis with full control panel.	—	—	Included
Memory controller with 8K word Memory-Pacs, Types CMC9001 and CMC9002 for up to 64K.	—	—	Required
Multiple Device Controller (MDC9101)	Required	Required	Required

The following is a list of Level 6 equipment options, components, accessories, peripherals, communications devices, cabinets, and the power distribution unit.

Central System

CPS9450	Model 6/34, 32K Memory
CPS9460	Model 6/36, 64K Memory
CPS9461	Model 6/36, 64K Memory (10 slot)
CMC9001	First Memory Controller with Parity 8K word Memory-Pac or
CMC9002	First Memory Controller with EDAC 8K word Memory-Pac
CMM9001	Second Memory, with Parity, Up to three 8K word Memory-Pacs can be added.
CMM9002	Second Memory with LEDAC. Up to three 8K word Memory-Pacs can be added.
PS9002	Memory Save and Auto restart, for up to 64K words, for Rack mountable unit.
PS9001	Memory Save and Auto restart, for up to 64K words, for Table Top Model

Central System General Options

CPF9401	Watchdog Timer
CPF9402	Multiprocessor Option
CAB9401	4 Slot Megabus Expansion chassis with Power Supply
CAB9402	9 Slot Megabus Expansion chassis with Power Supply
GIS9001	General Purpose DMA Controller

Central System Components and Accessories

CPU9401	6/34 Processor Board
CPU9402	6/34 Processor Board with Watchdog Timer
CPU9403	6/36 Processor Board
CPU9404	6/36 Processor Board with Watchdog Timer
CPU9405	6/36 Processor Board with Multiprocessor Option
CPU9406	6/36 Processor Board with Watchdog Timer and Multiprocessor Option
CPF9403	6/34 Control Panel
CPF9404	6/36 Control Panel
PSS9401	Power Supply for 4 or 5 slot Megabus chassis (requires two power supplies for 9 or 10 slot chassis).
CBL9101	ASR-33 Cable with connectors[a]
CBL9102	KSR-33 Cable with connectors[a]
CBL9103	CRT Console Cable with connectors[a]
CBL9104	30 CPS Console Cable with connectors[a]
CBL9105	Diskette Cable with connectors[b]
CBL9107	Serial Printers Cable with connectors[c]
CBL9108	Line Printers Cable with connectors[c]
CBL9106	Card Readers Cable with connectors[d]
Controller	Multiple Device Controller (MDC)

Console

TTU9101	ASR-33, Teleprinter Console[a]
TTU9102	KSR-33 Teleprinter Console[a]
DKU9101	CRT (TTY) Keyboard Console[a]
TWU9101	30 CPS Keyboard Telewriter Console (KSR)[a]
KCM9101	Device PAC for Keyboard Console

Diskettes

DIU9101	Single Diskette, Rackmounted Unit[b]
DIU9102	Dual Diskette, Rackmounted Unit[b]
DIM9101	Device-Pac for Diskette

Cartridge Disk

CDU9101	Cartridge Disk (rackmountable) 2.5 million bytes
CDU9102	Cartridge Disk (rackmountable) 5.0 million bytes
CDU9103	Cartridge Disk (rackmountable) 5.0 million bytes
CDU9104	Cartridge Disk (rackmountable) 10.0 million bytes

Printers

PRU9101	Serial Printer, 60 LPM, 64 character set
PRU9102	Serial Printer, 60 LPM, 96 character set
PRF9101	Serial Printer Pedestal
PRM9101	Printer Device-Pac
PRU9103	Line Printer, 240 LPM, 96 character set[c,e]
PRU9104	Line Printer, 300 LPM, 64 character set[c,e]
PRU9105	Line Printer, 480 LPM, 96 character set[c,e]
PRU9106	Line Printer, 600 LPM, 64 character set[c,e]
PRM 9101	Printer Device-Pac
PRF9102	12 Channel VFU

Card Equipment

CRU9101	Punched Card Reader 300 CPM[c,d]
CRU9102	Punched and Marked Card Reader 300 CPM[d,f]
CRU9103	Punched Reader[d,f]
CRU9104	Punched and Marked Card Reader[d,f]
CRF9101	51-Column Card Option
CRM9101	Card Reader Device-Pac

Communications

MLC9101	Multiline Communications Processor with Communications-Pacs for 8 Asynchronous Lines up to 9.6 KB each
MLC9102	Multiline Communications Processor with Communications-Pacs for 8 Synchronous Lines Up to 10.8 KB each
DCM9103	Multiline Communications Processor[g,h,i,j,k]
DCM9101	Communications-Pac, 2 Asynchronous Lines up to 9.6 KB each
DCM9102	Communications-Pac, 1 Asynchronous Line up to 9.6 KB
DCM9103	Communications-Pac, 2 Synchronous Lines up to 10.8 KB
DCM9104	Communications-Pac, 1 Synchronous Line up to 10.8 KB
DCM9105	Communications-Pac, 1 Broadband Line up to 72 KB

Cabinets and Power Distribution Unit (PDU)

CAB9001	Table Top Enclosure (CPS)
CAB9002	Diskette Table Top Enclosure
CAB9003	60" Rackmounted Unit with all Panels and Doors
CAB9004	60" Rackmounted Unit without Panels and Doors
CAB9005	Door – Upper Front
CAB9006	Panel – CPS Front Cover
CAB9007	Door – Lower Frton
CAB9008	Panel – One Side (Two Required)
CAB9009	Door – Rear
CAB9010	Extension – Table Wing
PSS9004	Power Distribution Unit (PDU) for Rack mountable Units by customer

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[a] KCM9101 Device-Pac is a prerequisite for Keyboard Console

[b] DIM9101 Device-Pac is a prerequisite for Diskette

[c] PRM9101 Device-Pac is a prerequisite for Serial and Line Printers

[d] CRM9101 Device-Pac is a prerequisite for Card Readers

[e] PRF9102 12 Channel VFU is a prerequisite for Line Printers

[f] CRF9101 51-column Card Option

[g] DCM9101 Communications-Pac is a prerequisite for 2 Asynchronous Lines up to 9.6 KB each

[h] DCM9102 Communications-Pac is a prerequisite for 1 Asynchronous Line up to 9.6 KB

[i] DCM9103 Communications-Pac, is a prerequisite for 2 Synchronous Line up to 10.8 KB

[j] DCM9104 Communications-Pac, is a prerequisite for 1 Synchronous Line up to 10.8 KB

[k] DCM9105 Communications-Pac, is a prerequisite for 1 Broadband Line up to 72 KB

DEVICE LAYOUT DESCRIPTION

Layout

Level 6 offers the customer three unit configurations and an operators extension table:

- Rackmoutable Unit
- Tabletop Unit
- Rackmounted Unit (by Honeywell)
- Operators extension table

Rackmountable units include the same physical devices as the basic rackmounted units, but are meant to be installed in a customer supplied (Rackmounted Electronics Terminal Manufacturers Association) RETMA cabinet. The individual module devices are housed in several types of enclosures with heights of 13.4 cm (5-1/4″), 17.7 cm (7″) and 25.4 cm (10-1/2″) with side-mounted fittings permitting it to slide into a standard 48.2 cm (19″) RETMA cabinet (see Figure 8-1).

The tabletop module devices in some cases contain the same physical, mechanical and electrical characteristics as the rackmountable module devices except that they are self contained with dress panels, tops, back and sides which can be placed on desks, tables or other flat surface support areas (see Figure 8-2).
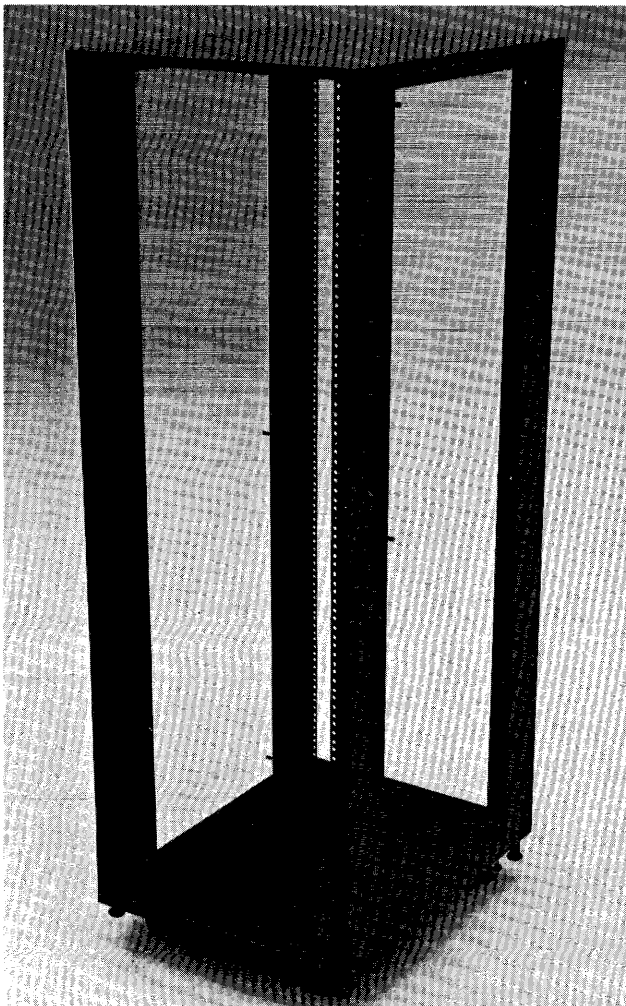
Figure 8-1. Typical RETMA Cabinet Application
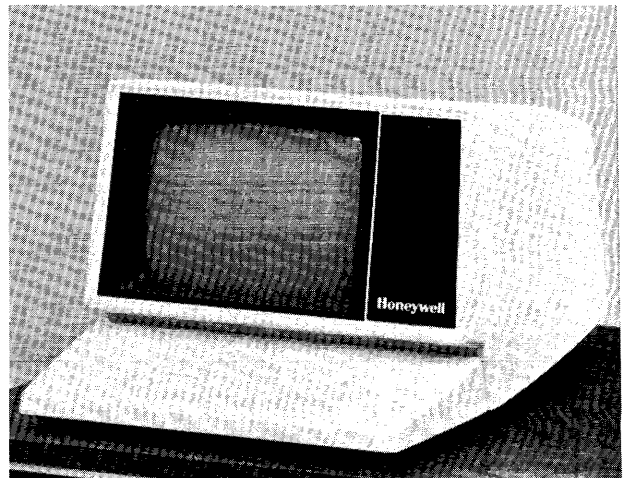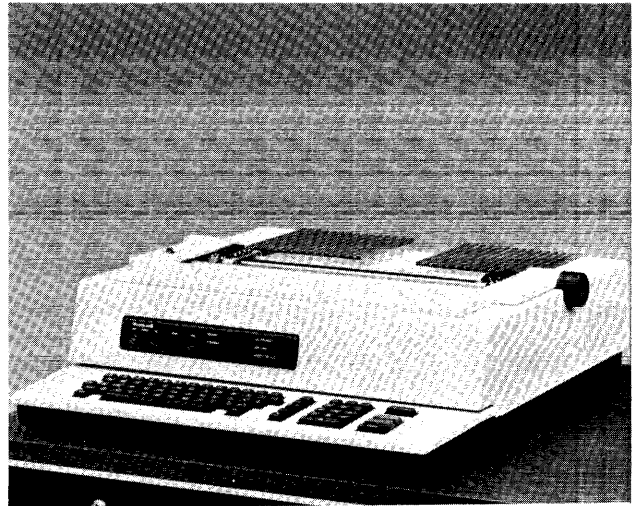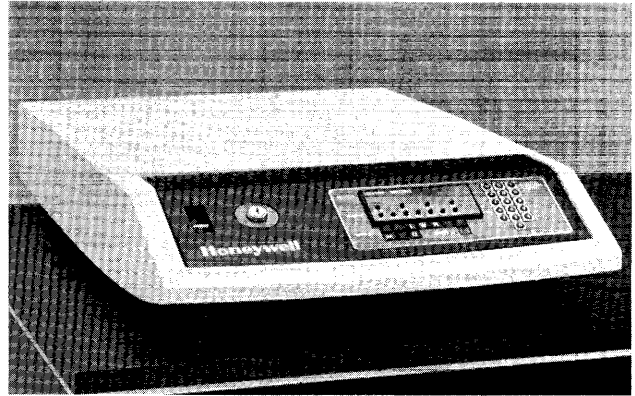
Figure 8-2. Typical Tabletop Models
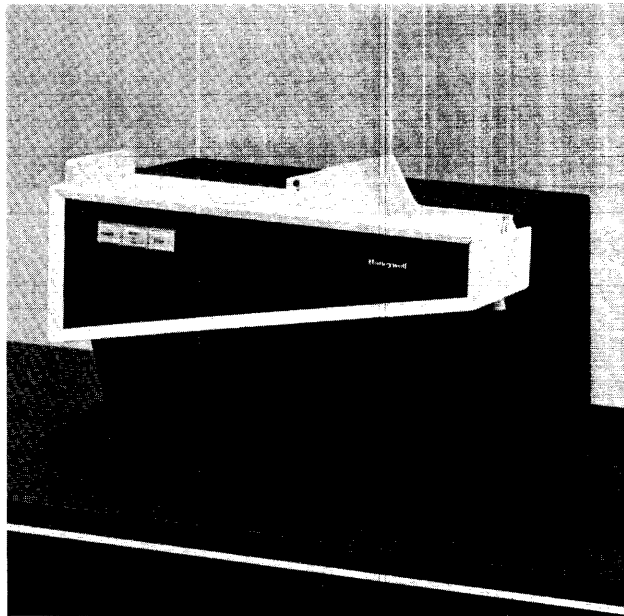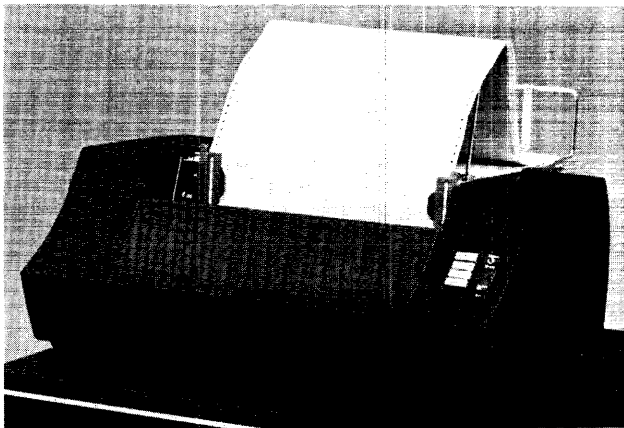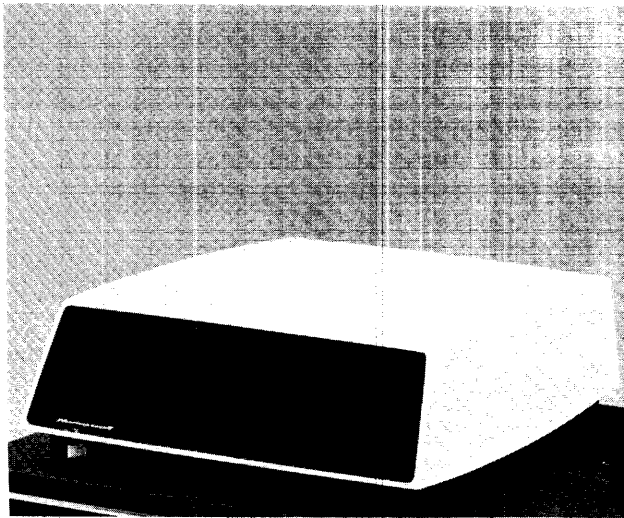
Figure 8-2. (cont). Typical Tabletop Models

The rackmounted unit Type CAB9003/ CAB9004 (by Honeywell) is packed so as to be complete in everyway. All module devices are positioned and installed in their proper locations based on the standard heights of 8.8 cm (3-1/2″), 13.4 cm (5-1/4″), 17.7 cm (7″) and 25.4 cm (10-1/2″). The PDU (a 13.4 cm (5-1/4″) height module is in position A and is predetermined cabinet slot. Also available are same-size, blank, front dress panels used for fronts until upgraded module devices are ordered (see Figure 803).
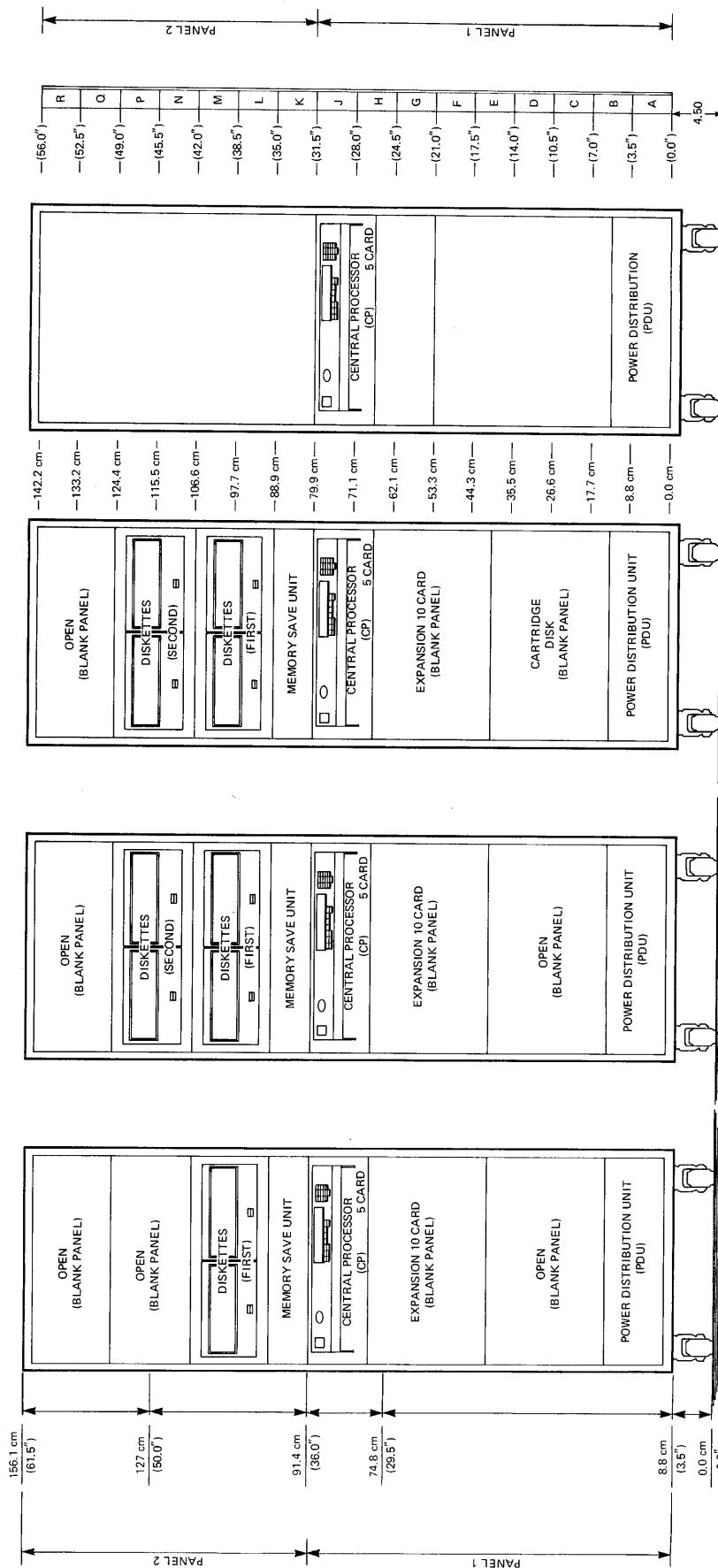
Figure 8-3. Typical Rackmountable Unit Configuration Plan Location for Models 6/34 and 6/36

The rackmounted unit provides the customer a complete package buildup within the 152 cm (60″) cabinet for versitility to grow not only in free-standing cabinets but to add floor-type add-on peripherals such as; consoles, teleprinters, printers, etc.

The layout of the various assemblies such as; CPS, memory, PDU (standard position), diskettes, cartridge disks, terminals etc. are mounted in predetermined locations based on sensible and workable arrangements within the rackmounted unit. Some assemblies must be close to each other for speed reasons, whereas other assemblies must be located at various points along the Megabus because of timing restrictions. Operation assemblies are located at certain heights for ease of operator use and some assemblies equally positioned in other 152 cm (60″) cabinets (see Figure 8-4 and Table 8-2).

Open Blank Panel

Single and Dual
Diskettes
DIU9101 and DIU9102

Memory Save
and Autorestart
PSS9001 or PSS9002

Central Processor
CPS9450
CPS9460
CPS9461

Control Panel
CPF9403

Expansion Area
for:
    ID Cards

1st Cartridge
Disk CDU9101
through CDU9104

Power Distribution
Unit (PDU)
PSS9004
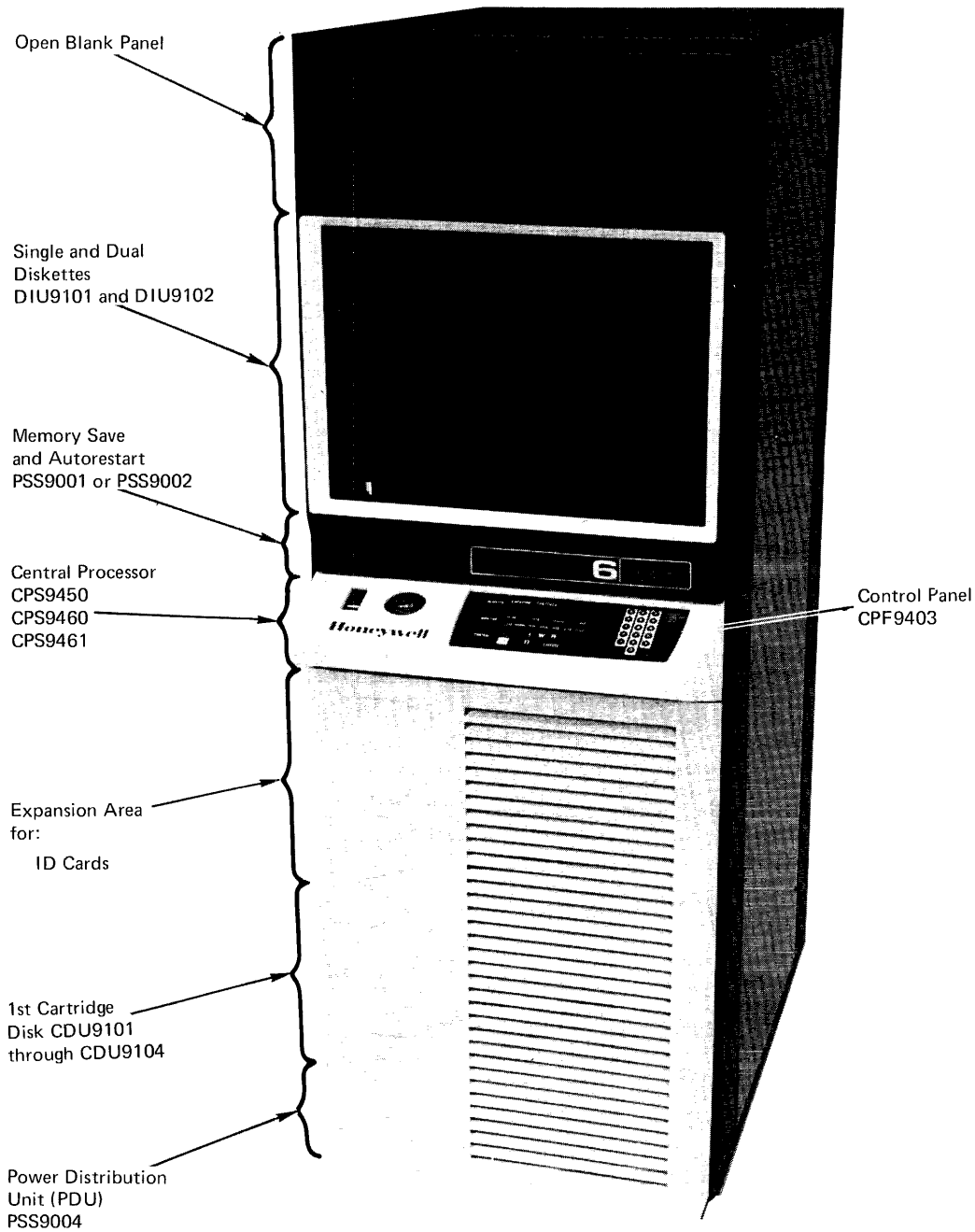
Figure 8-4. Standard Rack Assembly Locations

The operators extension table option Type CAB9010 is offered to the customer's operator for several operational reasons. When additional work surface is a necessity and when configuration necessitates tabletop module devices such as: CRT console, serial printers. Diskettes, Cartridge Disk, and Card Readers be placed nearby for operators convenience.

In addition the operators extension table allows not only tabletop placement of devices but also provides for freestanding peripherals to be close to left hand side of operator for monitoring.

Summarized in Table 8-3 are the device module locations for the various type of unit configurations including operators extension table.

Typical installation layouts and location for rackmountable units for Model 6/34 and 6/36 are presented in Figure 8-5, based on Table 8-2. For each model and the *individual*, freestanding device specifications see Table 8-6. The typical rackmountable unit configured plan location for Models 6/34 and 6/36, Figure 8-3, indicates the two panel levels, predetermined cabinet unit heights, cabinet unit locations (both in metric and inches) and cabinet unit positions (A through R, without I and O alphas) for quick reference in locating device modules in small to large configurations. Individual specifications (see Table 8-6) for each device will allow you to update selected system by adding to or deleting from the equipment complement as needed, thus requiring minimal rework. Blank worsheets, and templates, metric conversions are provided at the end of this section.

The symbols in the layouts that indicate the position and type of ac power connectors and receptacles are defined in Table 8-5.

When calculating the floor area required for the equipment, plan for columns, power facilities, air conditioning equipment, and storage facilities not included in the layout. Always keep in mind the aesthetic appearance of the installation. In laying out a configuration, do not exceed the standard cable limitations given in Table 8-6. The required access to each minicomputer device for operators and/or maintenance engineers is indicated in the individual device specifications by a dashed line.

TABLE 8-3. TYPE AND UNIT CONFIGURATION LOCATIONS

Type Number	Rackmountable	Tabletop	Rackmounted	Extension Table Wing	Freestanding
CPS9450 Model 6/34 (5 slot chassis)	Yes	Yes	Yes	Yes	N/A
CPS9460 Model 6/36 (5 slot chassis)	Yes	Yes	Yes	Yes	N/A
CPS9461 Model 6/36 (10 slot chassis)	Yes	No	Yes	No	N/A
PSS9001/PSS9002 Memory Save	Yes	Yes	Yes	Yes	N/A
PSS9004 Power Distribution Unit (PDU)	Yes	No	Yes	N/A	N/A
TTU9101 ASR-33	N/A	N/A	N/A	N/A	Yes
TTU9102 KSR-33	N/A	N/A	N/A	N/A	Yes
TWU9101 Keyboard Typewriter	N/A	Yes	N/A	Yes	N/A
DKU9101 CRT	N/A	Yes	N/A	Yes	N/A
DIU9101 Single Diskette DIU9102 Double Diskettes	Yes	Yes	Yes	Yes	N/A
Cartridge Disc CDU9101 through CDU9104	Yes	Yes	Yes	N/A	N/A
PRU9101 and PRU9102 Serial Printer	N/A	Yes	N/A	Yes	Yes (PRF9101 Pedestal Required)
PRU9103 through PRU9106 Line Printers	N/A	N/A	N/A	N/A	Yes
CRU9101 through CRU9103 Card Reader	N/A	Yes	N/A	Yes	N/A
MLC9101 and MLC9102 Multiline Comm. Proc.	Yes	N/A	Yes	N/A	N/A

EXTENSION
TABLE WING
CAB7010
(BY CUSTOMER)

CENTRAL
PROCESSOR
CPS9450
CPS9460
CPS9461
F

CRU9101
THROUGH
CRU9104
CARD READERS
F

PRF9101
PRINTER
STAND

PRU9101
AND
PRU9182
SERIAL PRINTERS
F

CHAIR
BY
CUSTOMER

TTU9101
TTU9102
ASR33 OR KSR33
TELEPRINTERS
F

NOTES
a RACEWAY IS
AVAILABLE. SEE
PAGE A-2.

15.34 SQ.M.
165.2

412.1 cm
(162¼")

372.0 cm
(146½")

Figure 8-5. Typical System Layout

Honeywell

–ELECTRICAL–

GENERAL:

A. Ac power will be supplied by the customer based on the requirements listed in these specifications.

B. The electrical power source will be independent and isolated from all other loads.

C. An allowance for expansion is recommended. (See Sheet 2 for specifications.)

D. All wiring must be installed in accordance with the National Electrical Code and other local ordinances. Costs for installing and/or modifying will be borne by the customer.

E. The electrical ground source shall be free of ground loops.

REQUIREMENTS:

A. The customer will supply and install in the computer room all AC receptacles indicated in the system layout and in Table 8-6 for individual unit specifications.

B. AC Power requirements for Level 6 Systems central processor cabinet and expansion cabinets (add-ons) (either of the following sources may be utilized):

1. Input voltage should be from a 208 VAC RMS, 60 Hz, three-phase (one phase not used), 4-wire plus ground source with 24A at 208 VAC RMS, or

2. 240 VAC RMA center-tapped (neutral 60 Hz, single-phased, 3-wire, plus ground source. If 240 is used, the Hubbell 25414 or 25403 (customer supplied) must be wired with the high lines ("hot" wires) connected to pins X & Y and the neutral center tap connected to pin W.

3. Loading on the input lines will be from phase to neutral on two phases only. Maximum load current per phase will be 24A; there is no internal provision or procedure for balancing the load. The unused phase is truncated at the input connector. Cabinet containing central processor requires a drop; second cabinet (options) is slave to central processor cabinet. If third cabinet is required, another drop is used. Fourth cabinet, if required, is slaved to third. All cabinets requiring drops receive a "primary power contactor pick" voltage from central processor cabinet. No growth factor required.

C. Listed below are the electrical specifications for the Level 6 System peripherals.

1. Load – 12.42 KVA for peripherals only.

2. Voltage – 120/208 ± 10%, 3-Phase (only use two phases of the three phases).

3. Frequency – 60 Hz ± 1/2 Hz

4. Phase and number of wires as indicated.

NOTE: The equipment neutral wire must not be connected to building ground except at power source (transformer, or building service entrance).

In the unusual cases wherein the power company does not regulate its power within the above tolerances and/or your facility imposes heavy loads on their substations, you are advised to furnish and install a voltage regulator.

Interconnecting cables between units shall be protected from mechanical injury. Product line raceways can be purchased through your Honeywell sales representative if raised flooring is not used. Raceway specifications are available from your Honeywell site planning engineer. The cost of supplying and installing raceway will be borne by the customer.

Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 1)

−AIR CONDITIONING−

GENERAL:

A. The heat dissipation figures listed on Sheet 2 for each unit *do not include* the heat gain from other sources: namely, lighting, people, building transmission, and fresh air loads. The total, however, allows for a 30% growth in equipment and should be considered when figuring the size of the air-conditioning system.

B. Check NFPA-75 for fire protection information.

C. Costs for installing and/or modifying air-conditioning will be borne by the customer.

REQUIREMENTS:

A. Listed below are the air-conditioning specifications.

   1. Cooling required for equipment only 3.385 kcal/hr or 3.933 watts (13435 Btu/hr or 1.1 tons).

   2. Temperature measured at input air of minisystem units − $23°C \pm 3°C$ ($73°F \pm 5°F$).

   3. Relative humidity − 40 to 60%.

   4. Filtration − Normal, unless environment is subjected to corrosive gases, salt air, or other unusual conditions, in which case special filtering will be required. If mechanical filters are used, their efficiency rating shall not be less than 20%.

   5. It is strongly recommended that the computer room air-conditioning system be a separate system because computer rooms require year-round cooling. (Window-type air-conditioning units are not recommended.)

REFERENCES:

For additional information and recommendations concerning the above subjects, as well as acoustical ceilings, fire control, cables, etc., contact your local Sales Representative or Field Engineer.

**Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 2)**

Qty.	Device	Marketing Identifier	Electrical Power		Receptacles (Symbol/type)		Heat Gain (kcal/hr or watts)	Weight (kg)	Dimensions W/D/H (cm)	Cables (m)	
			(kVA)	(amps)						ac	dc
1	Central Processor System: Cabinet #1 CP - 64K	CPS9460 CAB9003	Electrical Notes: A & B 8.64	30	Ⓐ	A	2016 2343	226.0	52.0/76.2/156.2 Control Panel Overhang	1.8	15.2
1	Extension-Table Wing	CAB9010	–	–	–		–	29.9	xxx/92.2/xxx		
1	Control Panel	———	within above cabinet					–	–	–	–
1	Memory Save and Artorestart	PSS9110	within above cabinet					–	–	–	–
2	Double Diskette	DIU9102	within above cabinet					–	–	–	–
1	Cartridge Disk Unit	CDU9101	within above cabinet					- -	–	–	–
1	ASR33 Teletypewriter	TTU9101	0.26	15	Ⓕ	F	94 / 109	25.4	55.8/46.9/66.0	1.8	7.6
1	Serial Printer	PRU9101	0.45	15	Ⓕ	F	340 / 395	54.4	71.1/55.8/34.2	2.4	15.2
1	Serial Printer Pedestal	PRF9101	–	–	–	–	–	23.6	71.1/55.8/66	–	–
1	Card Reader	CRV9101	0.21	15	Ⓕ	F	154 / 179	15.8	49.5/38.1/34.2	1.8	15.2
	Total		9.56	–	–		2604 / 3026	375.1	–	–	–
	30% Growth Factor		2.86	–	–		781 / 907	112.5	–	–	–
	GRAND TOTAL		12.42	–	–		3385 / 3933	487.6	–	–	–

Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 3)

Qty.	Device	Marketing Identifier	Electrical Power		Receptacles (Symbol/type)		Heat Gain (kcal/hr or watts)	Weight (kg)	Dimensions W/D/H (cm)	Cables (m)	
			(kVA)	(amps)						ac	dc
1	Central Processor System:	CPS9460	Electrical Notes: A & B 8.64	30	Ⓐ	A	(8000)	500	20½/30/61½ Control Panel Overhang xxx/36¼/xxx	6	50
	Cabinet #1	CAB9003									
1	CP - 64K Extension-Table Wing	CAB9010	–	–	–		–	66	24/30/30	–	–
1	Control Panel	―――	within above cabinet					–	–	–	–
1	Memory Save and Autorestart	PSS9110	within above cabinet					–	–	–	–
2	Double Diskette	DIU9102	within above cabinet					–	–	–	–
1	Cartridge Disk Unit	CDU9101	within above cabinet					--	–	–	–
1	ASR33 Teleprinter	TTU9101	0.26	15	Ⓕ	F	(375)	56	22/18½/26	6	25
1	Serial Printer	PRU9101	0.45	15	Ⓕ	F	(1350)	120	28/22/13½	8	50
1	Serial Printer Pedestal	PRF9101	–	–	–	–	–	52	28/22/26	–	–
1	Card Reader	CRV9101	0.21	15	Ⓕ	F	(610)	35	19½/15/13½	6	50
	Total		9.56	–	–		10335	82.9	–	–	–
	30% Growth Factor		2.86	–	–		3100	24.8	–	–	–
	GRAND TOTAL		12.42	–	–		13435	10.87	–	–	–

Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 4)

SPECIFICATIONS

The location of the minicomputer facility should be selected with regard not only for the decor space, clearance, operation of the minicomputer and its peripherals, but also for air conditioning, and electrical power. These considerations apply equally to new and old buildings.

Decor

Choice of materials and finishes used in the interior design of the area must take into account the structural and maintenance considerations listed under site facilities at the end of this section. Paint for example, should not chalk, powder, or flake, to avoid unwanted dust.

The finish of the Honeywell equipment is durable, attractive, and easy to maintain. The devices are *black* and *white* with colored accent panels. Standard accent color is blue; red and yellow panels are available for an extra charge with a Request for Price Quotation (RPQ) from the Marketing Sales Representative. Table 8-4 lists standard and optional equipment colors.

Space Requirements

The floor area required is determined by the system's complement of equipment. Also, the system's floor space depends upon the shape of room, the number and locations of permanent walls, partitions, entrances and exits.

Storage facilities for media and other items necessary for system operation should be designed to minimize both the amount of area necessary and travel time between areas.

Consider the possibility of later expansion when you are selecting an area.

Clearance

Specific considerations involved in designing an efficient processing center vary from installation to installation. Five major considerations for space and specifications, however, apply:

- Do not underestimate growth potential. The trend is toward additional minicomputer uses, and this means additional equipment and, in turn, additional space.
- Make sure that the equipment is situated where Honeywell recommends (see page 8-11A) for the best operation and comfort.
- Deviations from the recommended environmental specifications (included in this section) can cause serious problems in the operation and maintenance of equipment.
- Power isolation and regulation are necessities particularly since growth in the amount of power may be required.
- Space for expansion must be allotted for at least one expansion cabinet.

Operation and Peripherals

Honeywell has determined the optimum minisystem arrangement of equipment at a site, based on efficient operation. Specific criteria include:

- The console is the center of operations. The operator while sitting at the console can swing left, right, or back and be able to easily access equipment from all the usual working locations.
- Aisles to and from system at least 92 cm (36") wide allow access to all peripherals,

TABLE 8-4. EQUIPMENT COLORS

Color	Manufacturers Chip Number	Honeywell Standard Chip Number		Honeywell Standard and Optional Accent Colors
		Aspect	Tab #	
Gothic Black		Spatter	003	Standard Colors
		Smooth	252	
Executive White		Spatter	703	
		Smooth	704	
Black Laminate	Nevamar LH-6-1 (L)	Leather	601	
White Laminate	Formica White 949	Smooth	600	
Caribbean Blue		Spatter	001	Optional Accent Colors
		Smooth	250	
Hunter Red		Spatter	004	
		Smooth	254	
Aztec Yellow		Spatter	005	
		Smooth	254	

media supplies, and any maintenance equipment that must fit through the aisles.
- The freestanding peripherals should be arranged according to the frequency of operator access.
- The displays of module devices, freestanding cabinets, and addon peripherals should be visable from the console.

After evaluating the possible areas, you should prepare 1:50 cm (1/4″ to 1′) equipment layouts for areas under consideration. Use the scaled template in this section (page 8-30) for this purpose. Page 8-11 indicates a maximum system layout accompanied by complete specifications (Table 8-6) and followed by a photograph to be used as an overall guide.

The site layout should show:

- Entries and exits from truck off loading point
- Adjacent corridors, ramps, and staircases
- Building columns and internal windows.
- Site storage and media storage areas
- Any under-floor or above-floor obstructions that affect installation or routing of interconnecting cables.
- Raceways at walkways (when used)
- Ac ground
- Ac load centers
- System ground point
- Communication terminals (if used)

The final layout must be approved by you, by the Marketing Representative and by Field Engineering.

Air Conditioning

Minicomputer equipment, like any other equipment that consumes electrical energy, produces heat. As a result, air conditioning is an important requirement in site planning. This is not just for personnel comfort; the equipment and system media can tolerate conditions only within certain limits. Temperature regulation, humidity control, and air filtration are all essential factors for the system. The central processor, rackmountable devices, and freestanding peripherals are internally cooled by blowers that circulate room air through louvers in the cabinetry.

Air intake and exhaust varies slightly from one device to another. In general, cool air is transferred through louvers from front to rear, side to side, along the bottom edge (in some units) and lower cabinet section where cables enter the devices. For proper regulation of the environment of the computer room, air conditioning is required.

The air conditioning system for the installation should be completely separate and completely automatic, regulating conditions measured at the equipment air intake within the following range:

System Air Conditioning Requirements

	Operating Conditions	Storage Conditions
Temperature (dry bulb)	20°C-26°C (68°F-78°F)	5°C-45°C (40°F-110°F
Relative Humidity	40%-60%	10%-80% (No Condensation)

The lower limit for relative humidity depends on the characteristics of the cards disk pack, and paper to be used and on personnel comfort. The upper limit is subject to the condition that no condensation form on the equipment.

To maintain operating conditions within these limits, Honeywell recommends design conditions of:

Temperature (dry bulb)	23°C (73°F) ±6°C (±10°F)
Relative Humidity	50%

The individual air conditioning specification for the CPS9450, CPS9460, and CPS9461 Central Processor and its associated attached memory when used within a RETMA cabinet, separate rack, or an enclosure (by customer) is as follows:

Central Processor And Memory Air Conditioning Requirements

	Operating Conditions	Storage and Shipping Conditions
Temperature	0°C-50°C (32°F-122°F)	5°C-45°C (23°F-113°F)
Relative Humidity	5%-95% (No Condensation)	95%

This specification requirement serves for a *standalone environment only* for central processor and memory during its operation, storage, and shipping.

Three additional factors to consider are discussed below:

1. Humidity control will improve the performance of paper-handling devices (card readers, etc.) and avoid condensation and moisture. (The walls of the computer room should be adequately vapor sealed to reduce moisture problems.)

2. Filtration is essential to all areas to ensure clean air for the continuous and reliable operation of card readers, printers, and disk

devices. There are many sources of dirt, both from outside (clothes, shoes, dandruff, as well as the air supply) and within the room (magnetic oxide and paper dust produced by handling these materials on the system itself). However, provided the precautions are taken, the recommended standard of filtration, operating on the major source of dirt, has been found to ensure the satisfactory operation of card readers, printers and disk devices, and other sensitive devices, in association with the standard routine for cleaning these devices individually. It is relatively simple to filter the air to a good standard — a standard admittedly higher than the ultimate cleanliness of the room is likely to reflect — but it is not considered economic to go to extreme lengths in attempting to control the controllable sources of dirt when several uncontrollable sources still exist.

3. Air distribution, the means of delivering air to the computer room, should be flexible in design and not tied too closely to the proposed arrangement of the computer. In this way later changes can be effected without disruption of computer operation. Flexibility can be achieved with dampers and louvers to control the quantity and direction of air flow, or by use of a ventilated ceiling with certain panels masked off. In essence, the aim should be to condition the room and not the minicomputer.

Distribution of air to any other conditioned areas can be quite conventional, but the supply of air from the main air conditioner will need reheating if used directly.

After the system is installed and operating, the air supply dampers must be adjusted to balance the temperature throughout the area. Take care to locate and eliminate hot spots. It is suggested that an independent firm specializing in air balancing be employed to balance the computer room and provide certified test results to Honeywell Field Engineering.

In large facilities containing more than two systems, different design-point temperatures may exist in remote points of the room. This causes no problem as long as the temperature does not change more than $\pm 3°C (\pm 5°)$ at any one measurement point.

In determining the air conditioning requirements of your installation, consider:

1. The types of equipment that will be dissipating heat in the confined space. The central system and peripheral devices are cooled by air circulating fans that pull room air into the cabinet and exhaust the warmed air, usually out through the top or sides.
2. The heat gain and air conditioning loss through walls, ceilings, windows, doors, partitions, and lighting.

To find the number of tons of air conditioning required when kcal/hr (or Btu/hr) is known, use the formula:

$$\frac{kcal}{1000} \ or \ \frac{Btu/hr}{12,000} = tons \ of \ air \ conditioning$$

Continuous monitoring of the site's temperature and humidity is recommended as a way to save downtime. Recording instruments will indicate, for example, the extent and duration of any undesirable environmental conditions. The recorder used should satisfy the following criteria:

- The means of delivering air to the minicomputer area should not be tied too closely to the proposed layout of the equipment, in case of changes later. Flexibility can be achieved by using dampers and louvers to control the quantity and direction of air flow or by using a ventilated ceiling with certain panels masked off.
- Distribution of air to any other conditioned areas can be conventional, but the supply of air from the main air conditioner will need reheating if used directly. Small areas such as equipment and media storage areas can be conditioned by spillover air from the computer room, entering through suitable grilles or a doorway and then extracted back to the main air conditioners.

Air filtration is an essential adjunct to the regular cleaning regime to help ensure continuous and reliable operation of Level 6 systems.

To make the filtration system effective, seal all windows and control smoking in the area. In addition, provide for outdoor clothing to be removed and stored outside the area. Exert control on the supplier of continuous paper to leave only a minimum amount of loose paper dust adhering to the pack. The paper itself should not lose filler readily when it is handled.

Types of Systems

Whether you choose an overhead room air supply, an underfloor plenum supply, a combination system, or a freestanding air conditioner, you should use an experienced air conditioning engineer or consulting firm before designing the conditioning system. These specialists can assess the requirements for your installation. Window air conditioning units are not recommended because they are designed mainly for summer, not year-round cooling. A brief description of each type of system follows.

- Overhead Supply — Overhead ducts and diffusers supply cooled air, which is returned to the unit by means of the cooling plenum. Return registers are located above the devices. Careful attention must be given to the placement and design of the registers to achieve proper air balance within the room.
- Underfloor Supply — The area between the main floor and the raised floor can be used as a supply plenum. Cool air enters the computer area through floor registers and the raised floor cutouts (device cable entry). Warm air is returned through air grilles in the ceiling.
- Combination Supply — The area beneath the raised floor and the area above the suspended ceiling both supply cool air and return warm air.
- Freestanding — Freestanding air conditioners can be used for small and medium installations, provided the design can be adapted to the site. The underfloor plenum shown in Figure 8-6 is optional.

Electrical Power

You must furnish and install primary power for the system in accordance with the system specifications in Figure 8-7. It is also your responsibility to furnish and install the electrical equipment for the installation, including fittings, distribution panel, the raised floor device cutouts (if required), and transformer and voltage regulator (if required). Future expansion should always be considered, as provision for extra power facilities saves added installation costs later.

Many of the problems associated with computer operations originate in the primary ac power system. Disturbances such as electrical noise, power interruptions, and lightning must be factored into the plans for the power system for the user to have reasonable assurance that the computer system will perform satisfactorily and continue to operate. Close coordination with the electrical utility representative can lead to correction of potential problems originating in the utility system supplying power to the building. Many of the services and disturbances that can seriously affect an operation, however, are generated within the building itself. Your plant engineer, the electrical utility engineer, together must identify these disturbances and take steps to prevent possible adverse effects on the operation of the minisystem.

Power Source

The power source must have sufficient capacity to handle present computer loads and any loads likely to be imposed by future expansion of the system. The source must be independent of all other loads. That is, it must not provide power

Figure 8-6. Freestanding Air Conditioning System

A. From Single-Phase Transformer

B. From "Y" Connected Three-Phase Transformer

TO EQUIPMENT RECEPTACLES

NOTE: ABC Allowable power sources to PDUs

C. Equipment Ground Bus Bar (Bonded to Panel)
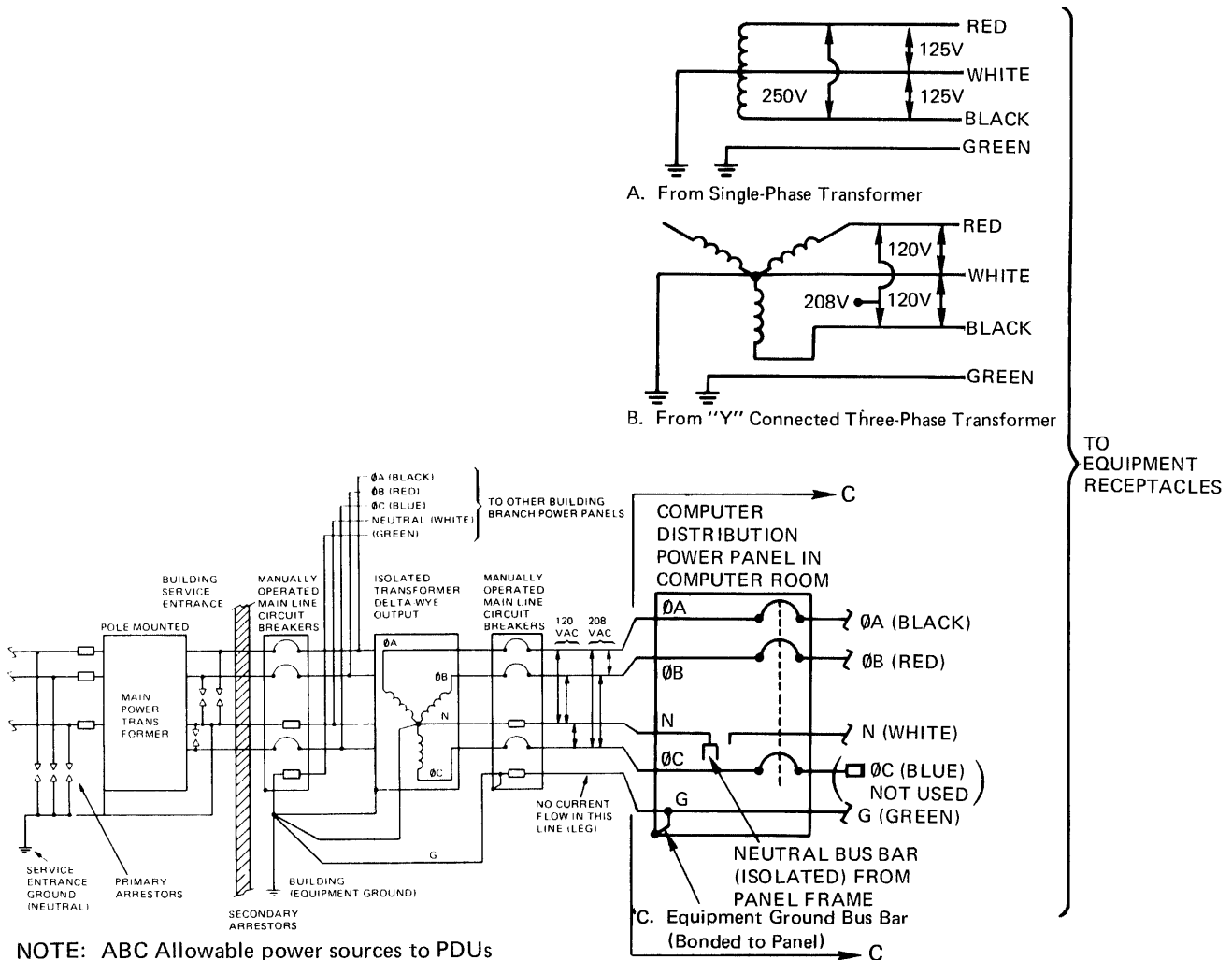
Figure 8-7. Schematic Showing Wye-Connection, Voltage, and Receptacle Relationship

for airconditioning equipment, convenience outlets, lighting, or office equipment. A separate building service entrance (or a main building service panel) input feeder connected to the computer distribution panel usually provides suitable power (see Figure 8-7).

To obtain isolation, a separate transformer and service drop is required to provide power to the computer system. The transformer must be adequate to handle the present load plus any future expansion. Many large buildings have multiple power systems with numerous service entrances supplied from the same transformer. An isolation transformer must be used to reduce noise and transient interference if you intend to connect to the available power.

The power that serves the system must meet the following requirements:

- The line voltage should rot have voltage transients greater than +6% or -14% from the nominal line to neutral of 120 volts.

- The line voltage should have total harmonic content of less than 6% of the power in the fundamental frequency.
- The line voltage must not have neutral grounded at any point in the entire power system supplying the computer except at the building service entrance or at isolation transformer when applicapable.
- The power source must be 120/208 volts, three-phase ±10% of the rated voltage, with a frequency tolerance of 60 Hz ±1/2 Hz and with a harmonic content within acceptable limits.

AC Power Sources for Types CPS9450, CPS9460 and CPS8461 Systems

Each cabinet contains a power distribution unit (PDU) (see page 8-10A) located at the bottom front of the cabinet when Central Processor (CP), Control Panel, Memory Save, and second Console ASR is figured in system complement. Each PDU requires its own connection to the primary power source (ac mains). A 6-foot power cable is attached to the rear of each PDU.

TABLE 8-5. RECEPTACLE SPECIFICATIONS

Type	Symbols	Amps	Volts	Phase and Wires	Mfg.	NEMA Std.	Unit Plug No.	Receptacle by Customer	Or	Connector by Customer
A	(A)	30	600	3Ø-5W	Hubbell or Arrow & Hart		25415	25403		25414
F	(F)	15	125	1Ø-3W	Hubbell		5266C	5262		5269
(By customer)	(⚑)	15	125	1Ø-3W	Hubbell		(By customer)	(By customer)		(By customer)

NOTE

The receptacle specifications are for your convenience. Refer to the manufacturer's catalog for complete compatibility as to exact equivalent. Honeywell assumes no responsibility for differences between manufacturers' receptacles.

The system is arranged so that energizing the power switch on the central processor drawer causes all outlets throughout the system to be energized, provided that the circuit breaker on each PDU is "on."

NOTE: De-energizing the circuit breaker in any cabinet removes power in that cabinet and all subsequent cabinets.

The permissible primary power to the Type CAB9003 system cabinet sources are as follows (permissible power sources for free-standing peripheral devices are described in Table 8-5.)

AC power requirements — either of the following sources may be utilized:

1. Input voltage should be from a 120/208 VAC RMS, 60 Hz, 3 phase, 4-wire, plus ground source with 24A at 208 VAC RMS, or
2. 240 VAC RMS center-tapped (neutral) 60 Hz, single-phase, 3-wire, plus ground source. If 240 is used, the Hubbell 25414 or 25403 (customer supplied) must be wired with the high lines connected to pins X & Y and the neutral center tap connected to pin W.
3. Loading on the input lines will be from phase to neutral on two phases only. Maximum load current per phase will be 24A; there is no internal provision or procedure for balancing the load. The unused phase is truncated at the input connector. The cabinet containing the central processor requires a drop; the second cabinet (options) is slave to the central processor cabinet. If a third cabinet is required, another drop is used. The fourth cabinet, if required, is slaved to the third. All cabinets requiring drops receive a "primary power contactor pick" voltage from the central processor cabinet.

The voltage shall be firm, varying by not more than ±10% of the rated amount, including transient and steady state. Where power is not regulated this closely, you are advised to furnish and install a voltage regulator.

Your Honeywell Marketing Representative or Field Engineer will answer your questions, but for redesign or highly technical problems, you should contact your electrical contractor or consulting engineering firm.

Power Distribution

If the electric power at the installation site is not of the required voltage, one or more transformers must be purchased and installed. A three-phase transformer or a bank of three single-phase transformers of identical rating and characteristics can be used. The capacity required depends upon the equipment complement and what is specified in the calculated installation specification.

The total system requires a power load balance calculation only when single-phase devices are included in the equipment. It is your responsibility to ensure that the phase loads are balanced (i.e., that the amperage is distributed evenly among the three phases of the system's power source). Load balancing prevents a large load from occurring on one phase of the transformer.

In a three-phase, wye-connected system with a grounded neutral, the phase imbalance currents flow in the neutral wire. This reduces the power system's efficiency, increasing power consumption and operating costs. High neutral ground currents can also generate noise levels that may be reflected back into the computer system. To avoid these problems, attention must be given to balancing the computer load throughout the system.

The feeder supplying power to the computer system should be protected by a mainline circuit breaker. The computer's distribution power panel should be located in an unobstructed, well-lighted area in the computer room.

Convenience Outlets

Auxiliary power, 120-volt, single-phase, 60-Hz wall outlets must be present in the computer area for the service engineers scopes, test equipment etc., vacuum cleaner, floor buffer, etc. Recommended circuit capacities are 15-20 amperes; individual outlet capacities are 15 amperes. The number and location of these outlets should be indicated on your approved system layout drawing. All convenience outlets in the computer room should be on a feeder separate from the computer system to prevent electrical noise interference.

Grounding

When providing the female receptacle or connectors for three-phase and single-phase devices, furnish and install a separate ground wire. Conduit, raceway, or other enclosures cannot be used for this purpose. For three-phase power, the fifth wire is to be used as the equipment ground; for single phase, the third wire. In both cases, the ground shall be connected to the metallic raceway system and/or the control panel, in accordance with the National Electrical Code (NFPA) No. 70.[a] The equipment ground shall *not* be connected to the neutral wire except at the building's main electrical service entrance. The ground wire, when installed in armor, cable sheath, conduit raceway, ladder tray, or other enclosure, should be sized according to the amperage specified in Table 250-95 of the National Electrical Code.[a] In no case shall it be smaller than number 12AWG.

WARNING

A five-wire connection (four-wire wye plus equipment ground) is used in Honeywell systems; the neutral is readily available. The neutral supplied is usually the white conductor in a multiconductor power cable.

The ac neutral must not be confused with protective (equipment frame) ground. The protective equipment ground — the green conductor in a multiconductor cable — prevents the buildup of dangerous voltages on equipment as protection for personnel. It ensures that any short circuit between a power phase and the cabinet draws enough current to trip the circuit's protective device immediately — rather than raising the potential of the equipment to a dangerous level. The ac neutral must never be connected to the frame of any equipment or to the protective ground.

Interconnecting Cables

Honeywell supplies and installs the necessary cables and raceway (if used) for the initial installation of the computer (with the exception of the ac cables). Since all cables are custom-made to specific lengths (see Table 8-6) it is essential that an approved system layout drawing be available at the proper time.

Any revisions of approved system layout drawings are considered on an RPQ (Request for Price Quotation) basis because a second cable order must be prepared.

Cables required for new, additional, or damaged equipment through the fault of Honeywell and within warranty period are supplied by Honeywell at no cost.

If cables are requested in other than standard lengths, the new cable lengths and the reason for the change must be specified on a Request Price Quote (RPQ) basis.

Power Receptacles and Connectors

You are required to install power receptacles and/or connectors in accordance with local electrical codes before delivery of the system. The locations and types of ac receptacles are given in Table 8-5 for each device. For quick reference in estimating a power load, the electrical specifications for each device are included in the summary table at the beginning of the section. The power loads listed do not represent the duty cycle, nor have they been derated to indicate the duty cycle. To meet the NFPA 70 Electrical Code, the primary distribution must be sized by the nameplate rating specified on the device.

The values shown for circuit breakers and wire sizes must also meet the NFPA 70 Code. Follow your local code if it requires larger sizes. The wires shown include the required "green wire" or safety ground conductor.

For a summary of receptacle specifications, see Table 8-5.

Figures 8-8 through 8-10 illustrate the ac-type male plugs that can be attached to the computer devices or to the power panel (depending on its location). The dimensions indicated for the connectors and receptacles are overall measurements and can be used in calculating subfloor clearances and clearances in walkways, cable channels, and raised floor cutouts.

Device Specifications

Models 6/34 and 6/36 consist of the following installation specifications for a system and are based on the individual device specifications in Table 8-6. If any devices or modules are added or deleted, the associated specifications should be revised by the customer, with copies sent to your Honeywell Marketing Representative. In this way, both the customer and Honeywell will have first-hand information for reworking total system requirements.

NO. 25415
SYMBOL (A)
TYPE A

Figure 8-8. Power Plug — Three-Phase, 30-Amp,
Five-Wire, 600V

NO. BY CUSTOMER
SYMBOL (F)
TYPE BY CUSTOMER

Figure 8-9. Power Plug — Single-Phase, 15-Amp,
3-Wire, 125V

NO. BY CUSTOMER
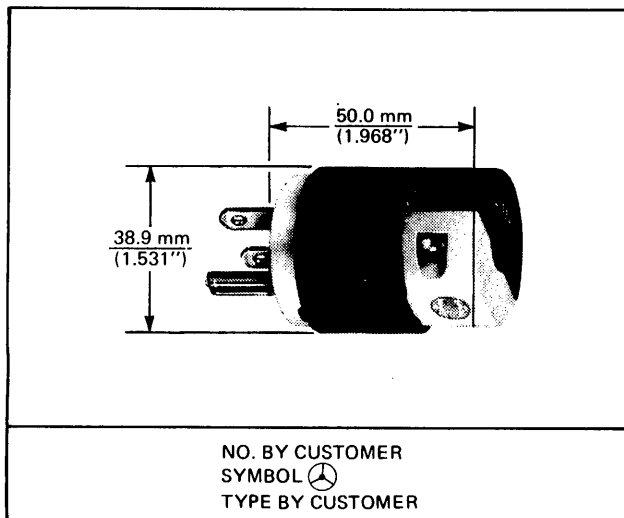SYMBOL (△)
TYPE BY CUSTOMER

Figure 8-10. Power Plug — Single-Phase, Straight
Blade, 15-Amp, Three-Wire, 125V

TABLE 8-6. CENTRAL PROCESSING SYSTEM SPECIFICATIONS

| Marketing Identifier | Description | Electrical Power | | | | Heat Gain kcal/hr or Watts (Btu/hr) | Dimensions W/D/H cm (in.) | Weight kg (lb.) | Cables (max.) m (ft.) | |
| | | KVA | Amps | Receptacle | | | | | ac | dc |
				Type	Symbol					
CPS9450 CPS9460 CPS9461	**Cabinet 1:** Central Proc. 64K Memory also includes CP cabinet fully loaded with power chassis and devices.	See Notes a and b	1/30	A	Ⓐ	$\frac{2016 \text{ or } 2343^b}{(8,000)}$	$\frac{52.0/76.2/156.2}{(20.5/30/61.5)}$ With control panel overhang: $\frac{xxx/92.2/xxxx}{(xxx/36.25/xxx)}$	$\frac{226^b}{(500)}$	$\frac{1.8}{(6)}$	$\frac{15.2}{(50)}$
CAB9010	Extension – Table Wing	—	—	—	—	—	$\frac{60.9/76.2/76.2}{(24/30/30)}$	$\frac{29.9}{(66)}$	--	--
CPS9450 or CPF9403	**6/34 Control Panel** (CP rackmountable) or (CP Tabletop CAB9001)	0.41	1/15	F	Ⓕ c	$\frac{403 \text{ or } 645}{(1,600)}$	$\frac{50.5/77.9/16.25^d}{(19.9/30.7/6.4)}$	$\frac{29.4}{(65)}$	$\frac{1.8}{(6)}$	$\frac{15.2}{(50)}$
CPS9460/ CPS9461 CPF9403	**6/36 Control Panel** (CPU rackmountable) or (CPU Tabletop CAB9001)	0.41	1/15	F	Ⓕ c	$\frac{403 \text{ or } 645}{(1,600)}$	$\frac{50.5/77.9/16.25^d}{(19.9/30.7/6.4)}$	$\frac{29.4}{(65)}$	$\frac{1.8}{(6)}$	$\frac{15.2}{(50)}$
CONSOLE SPECIFICATIONS										
TTU9101	ASR-33 Teleprinter	0.26	1/15	F	Ⓕ c	$\frac{94 \text{ or } 109}{(375)}$	$\frac{55.8/46.9/66}{(22/18.5/26)}$	$\frac{25.4}{(56)}$	$\frac{1.8}{(6)}$	$\frac{7.6}{(25)}$
TTU9102	KSR-33 Teleprinter	0.23	1/15	F	Ⓒ c	$\frac{94 \text{ or } 109}{(325)}$	$\frac{55.8/46.9/66}{(22/18.5/26)}$	$\frac{25.4}{(56)}$	$\frac{1.8}{(6)}$	$\frac{7.6}{(25)}$
TWU9101	Keyboard Typewriter	0.23	1/15	F	Ⓕ	$\frac{126 \text{ or } 156}{(500)}$	$\frac{57.15/52.07/19.05}{(22.5/26.5/13.1)}$	$\frac{31.7}{(70)}$	$\frac{1.8}{(6)}$	$\frac{15.2}{(50)}$
DKU9101	CRT (TTY)	0.10	1/15	F	Ⓕ	$\frac{252 \text{ or } 292}{(1,000)}$	$\frac{20.3/60.9/33.0}{(18/24/13)}$	$\frac{18.1}{(40)}$	$\frac{1.8}{(6)}$	$\frac{15.2}{(50)}$
	Keyboard	—	—	—	—	$\frac{\text{N/A within CRT}}{(\text{N/A within CRT})}$	$\frac{20.3/20.3/7.6}{(18/8/3)}$	$\frac{\text{N/A within CRT}}{(\text{N/A within CRT})}$	N/A	Allow 0.9m (3 ft.) Separation
DISKETTES SPECIFICATIONS										
DIU9101	Single Diskette (rackmountable or tabletop unit)	0.42	1/15	F	Ⓕ c	$\frac{85 \text{ or } 100}{(340)}$	$\frac{52.07/68.3/18.5^d}{(20.5/26.9/7.3)}$	$\frac{27.2}{(60)}$	$\frac{1.8}{(6)}$	$\frac{6}{(20)}$
DIU9102	Dual Diskette (rackmountable or tabletop unit)	0.84	1/15	F	Ⓕ c	$\frac{171 \text{ or } 199}{(680)}$	$\frac{52.07/68.3/37^d}{(20.5/26.9/14.6)}$	$\frac{54.4}{(120)}$	$\frac{1.8}{(6)}$	$\frac{6}{(20)}$
PSS9001 or PSS9002	**Memory Save and Autorestart** (rackmountable) or (tabletop)	0.42	1/15	F	Ⓕ c	$\frac{72 \text{ or } 84}{(285)}$	$\frac{44.7/59.9/8.8^d}{(17.6/23.6/3.5)}$	$\frac{22.7}{(50)}$	$\frac{1.8}{(6)}$	$\frac{10.7}{(35)}$
CARTRIDGE DISK SPECIFICATIONS										
CDU 9101 through CDU9104	Cartridge Disk Units	0.80	1/15	F	Ⓕ e	$\frac{290 \text{ or } 337}{(1,150)}$	$\frac{48.2/76.2/24}{(19/30/8.75)}$	$\frac{38.6}{(85)}$	$\frac{2.4}{(8)}$	$\frac{3.3}{(11)}$

TABLE 8-6 (cont). CENTRAL PROCESSING SYSTEM SPECIFICATIONS

PRINTER SPECIFICATIONS

Marketing Identifier	Description	Electrical Power				Heat Gain kcal/hr or Watts (Btu/hr)	Dimensions W/D/H cm (in.)	Weight kg (lb.)	Cables (max.) m (ft.)	
		KVA	Amps	Receptacle					ac	dc
				Type	Symbol					
PRU9101	Serial Printer (64 character set)	0.45	1/15	F	Ⓕ	340 or 395 (1,350)	71.1/55.8/34.2 (28/22/13.5)	54.4 (120)	2.4 (8)	15.2 (50)
PRU9102	Serial Printer (76 character set)	0.45	1/15	F	Ⓕ	340 or 395 (1,350)	71.1/55.8/34.2 (28/22/13.5)	54.4 (120)	2.4 (8)	15.2 (50)
PRF9101	Serial Printer Pedestal						71.1/55.8/66 (28/22/26)	23.6 (52)		
PRU9103 through PRU9106	Line Printers	0.58	1/15	F	Ⓕ	454 or 527 (1,800)	83.8/55.8/114.3 (33/22/45)	154.2 (340)	1.8 (6)	15.2 (50)

CARD EQUIPMENT SPECIFICATIONS

Marketing Identifier	Description	KVA	Amps	Type	Symbol	Heat Gain	Dimensions	Weight	ac	dc
CRU9101 through CRU9104	Card Reader	0.21	1/15	F	Ⓕ	154 or 179 (610)	49.5/38.1/34.2 (19.5/15/13.5)	15.8 (35)	1.8 (6)	15.2 (50)

COMMUNICATIONS SPECIFICATIONS

Marketing Identifier	Description							Weight	dc
MLC9101 through MLC9102	Multiline Communications Processor	Figured within Central Processor Unit						N/A	9.1 (30)

Note:
a. The permissible primary power to the Type CAB9003 system cabinet sources are as follows (permissible power sources for rackmountable, table top, rackmounted and free-standing peripheral devices are described below for these devices):
  1. 120/240V (nominal) ac, single-phase, center-tapped, two hot wires plus neutral and safety ground (see diagrams below). Each "hot" wire may carry up to 15 amps depending on units installed in cabinet (i.e., up to 4 KVA/cabinet).
  2. 120/208V (nominal ac – Any two of the three phases plus neutral and safety ground of a three-phase wye-connected power system (see diagram below). Note that current and KVA rating are the same as in (1) above.
  3. Loading on the input lines will be from phase to neutral on two phases only. Maximum load current per phase will be 24A; there is no internal provision or procedure for balancing the load. The unused phase is truncated at the input connector. The cabinet containing the central processor requires a receptacle the second cabinet (options) is slave to the central processor cabinet. If a third cabinet is required, another receptacle is used. The fourth cabinet, if required, is slaved to the third. All cabinets requiring receptacle receive a "primary power contactor pick" voltage from the central processor cabinet.
b. Figures include maximum cabinet requirements and power supply specifications.
c. Receptacles needed when tabletop installed, otherwise, plugs into PDU.
d. Dimensions shown are configured for tabletop units. For rackmountable, see page 8-10.
e. Cartridge Disk Units always plug into Power Distribution Unit (PDU).

Site Preparation Check List

For your use in final preparation of your system a check off list follows indicating standard site preparation requirements.

- Review site layout for room size and serviceability?
- Does the system have its own power source?
- Is proper system ground present? (see page 8-22)
- Is ac neutral wired properly?
- Are all receptacles for system devices installed?
- Are there temperature and humidity controls?
- Does the computer room have its own air conditioner sized to meet present and future load requirements?

- Are all wall outlets on a separate feeder line?
- Is the computer room prepared properly for minimum dust and maximum cleanliness?
- Does the computer room have recommended fire protection?
- Does the computer room have recommended emergency power off wiring?
- Is the equipment ground and neutral isolated at service entrance?
- If raised floor, are cable and ac cutouts complete?
- Is Honeywell floor raceway ordered and available. (Optional)
- Have phone lines and communications modem hardware been ordered and installed?

Supplies and Accessories

Honeywell markets a complete line of computer supplies and accessories. For more information, see the Honeywell *Computer Supplies Catalog*, Order No. BY62, or your Honeywell Marketing Representative.

References

In addition, to aid you in your system installation work, Honeywell has listed several companion handbooks that are available as outlined below.

- *ASHRAE Handbook*, American Society of Heating, Refrigeration, and Airconditioning Engineers, New York City, New York.
- *Honeywell Computer Supplies Catalog*, Order No. BY62.
- *National Electric Code*, National Fire Protection Association (No. 5, No. 75, and No. 90A), 470 Atlantic Avenue, Boston, Ma 02210.
- *Plant Engineering Handbook*, McGraw Hill, New York City, New York.
- *Surface Metal Raceways and Fittings Standard For Safety*, No. UL-5 *Electronic Data-Processing Units and Systems*, No. UL-478; Underwriters Laboratories, Inc. Chicago, Ill; New York; Santa Clara, California.

PHYSICAL PLANNING AIDS

The following pages present photo templates (dimensioned and without dimensions), 1:50 mm (1/4 in.) and 1.50 (1/4 in.) and a floor layout grid. Use the templates and grid to make a rough draft of the layout you have selected. The templates and grid enable you to simulate your chosen system and help reconcile the possible conflicting requirements of proposed or existing walls, doors, windows, aisles, and so on.

Before proceeding to duplicate a standard layout, you should review this section.

The letter "F" on the templates indicates the front of the device. The inside (bold) lines indicate the main portion of the device cabinetry; the outside (dashed) lines indicate the swing of the doors and area for drawers, together with the required clearances for servicing each device. Clearances can be overlapped since it is unlikely that service would be performed on two adjacent cabinets at the same time; overlapping provides a more workable and compact configuration.

The ac plug symbols, located close to the floor cutout of each device, indicate the approximate location in which the ac receptacle and/or connector is installed (see Table 8-5).

Use the blank installation specification and individual equipment calculation forms on pages and for updating the standard system specifications in this section.
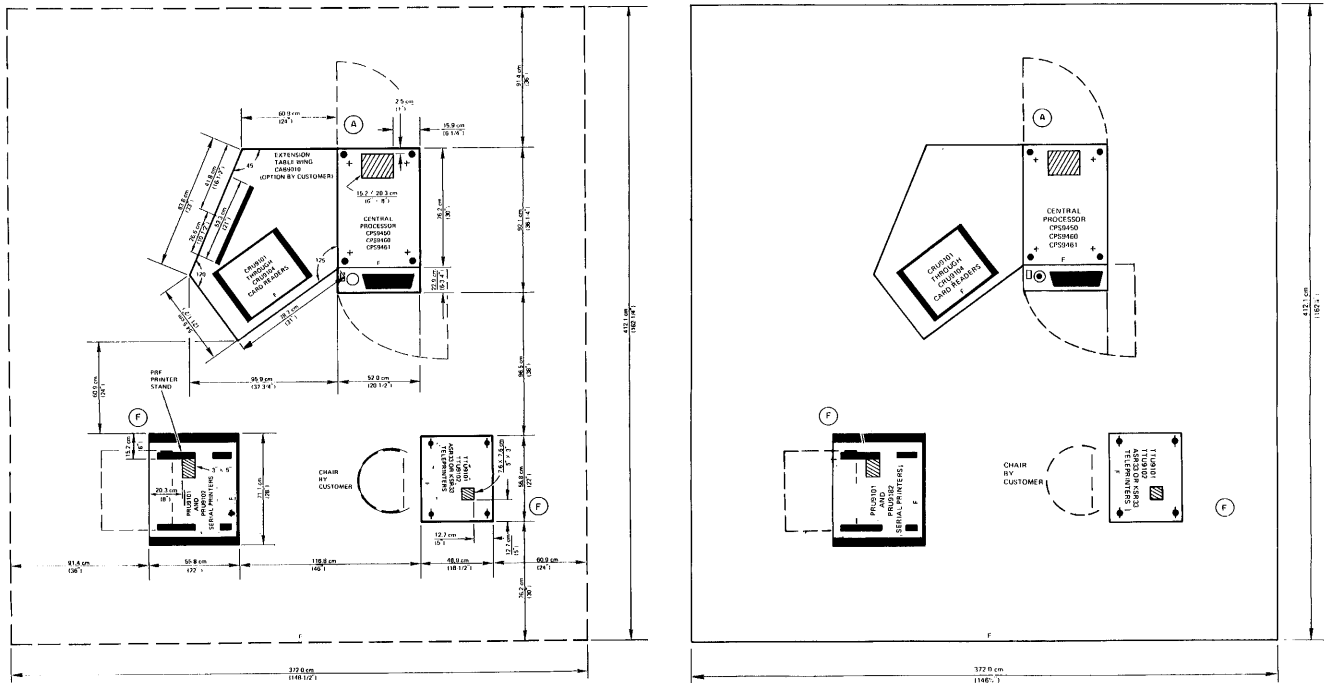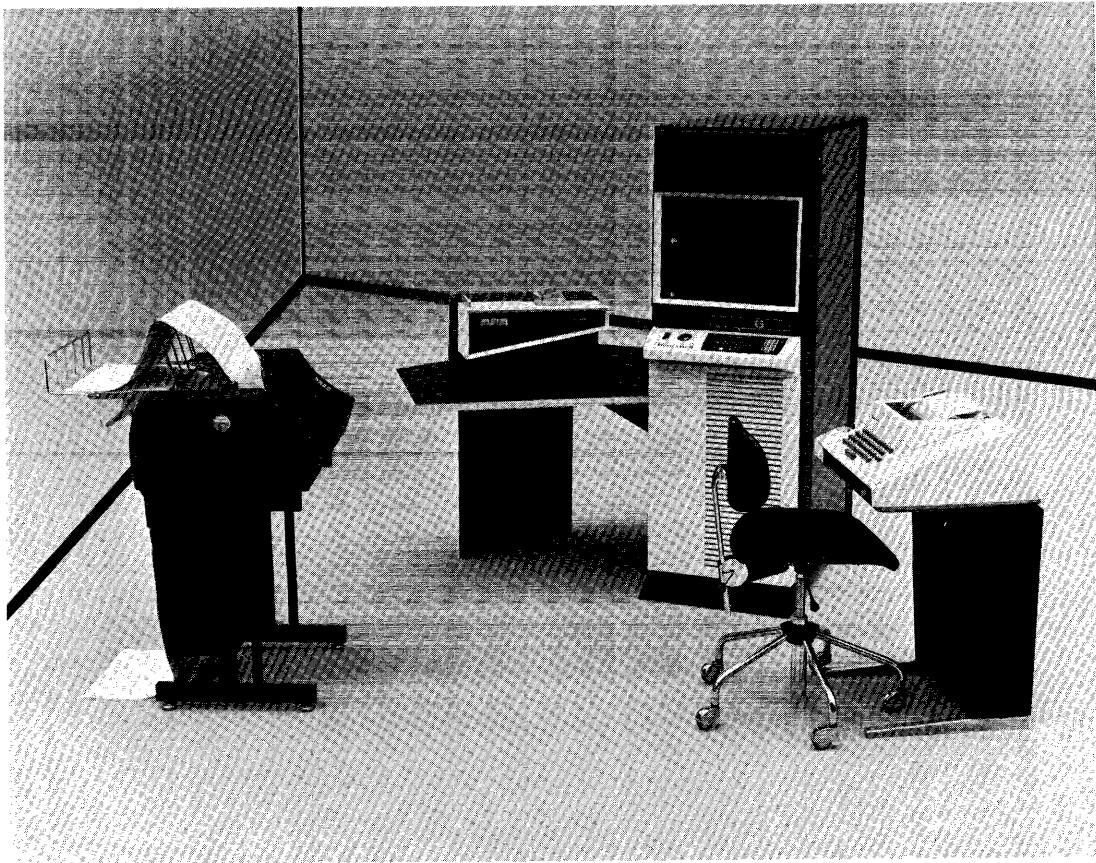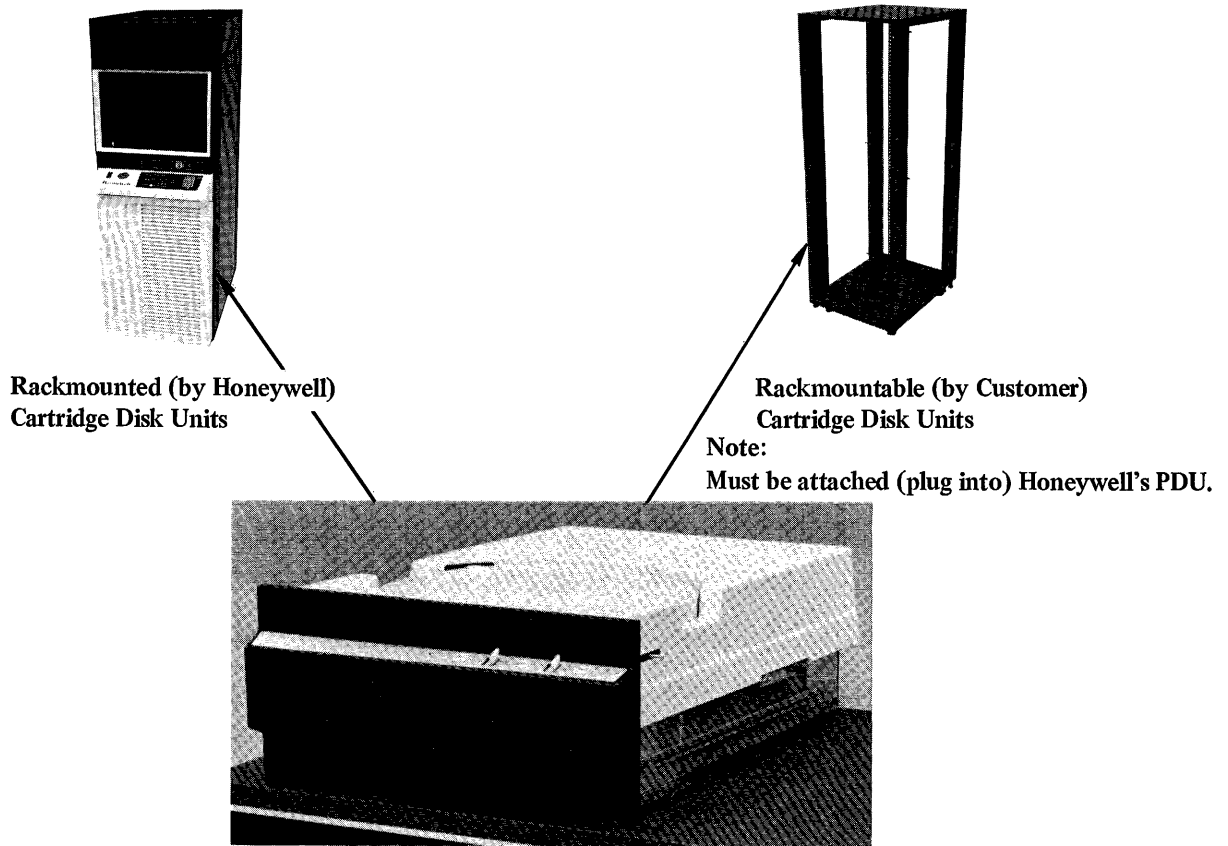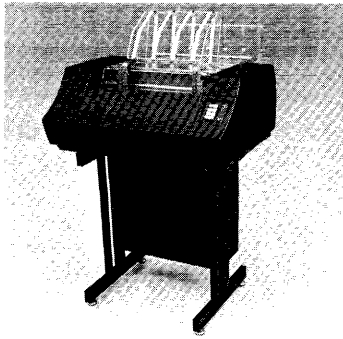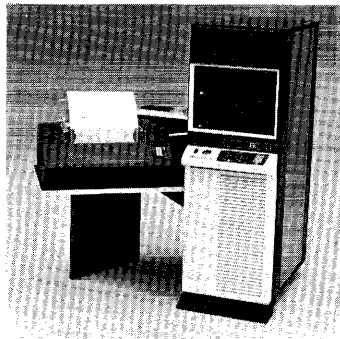
Figure 8-11. Typical Level 6 Layouts and Templates

**Rackmounted Unit (by Honeywell)**

Typical "RETMA" Cabinet for Rackmountable Units

Central Processor and Memory Save Rackmounted or Rackmountable

15.9 cm
(6¼")

2.5 cm
(1")

91.4 cm
(36")

15.2 X 20.3 cm
(6" X 8")

CENTRAL
PROCESSOR
CPS9450
CPS9460
CPS9461

F

76.2 cm
(30")

281.8 cm
(108¼")

99.0 cm
(36¼")

22.8 cm
(6.25")

(20½")

91.4 cm
(36")

F

CENTRAL
PROCESSOR
CPS9450
CPS9460
CPS9461
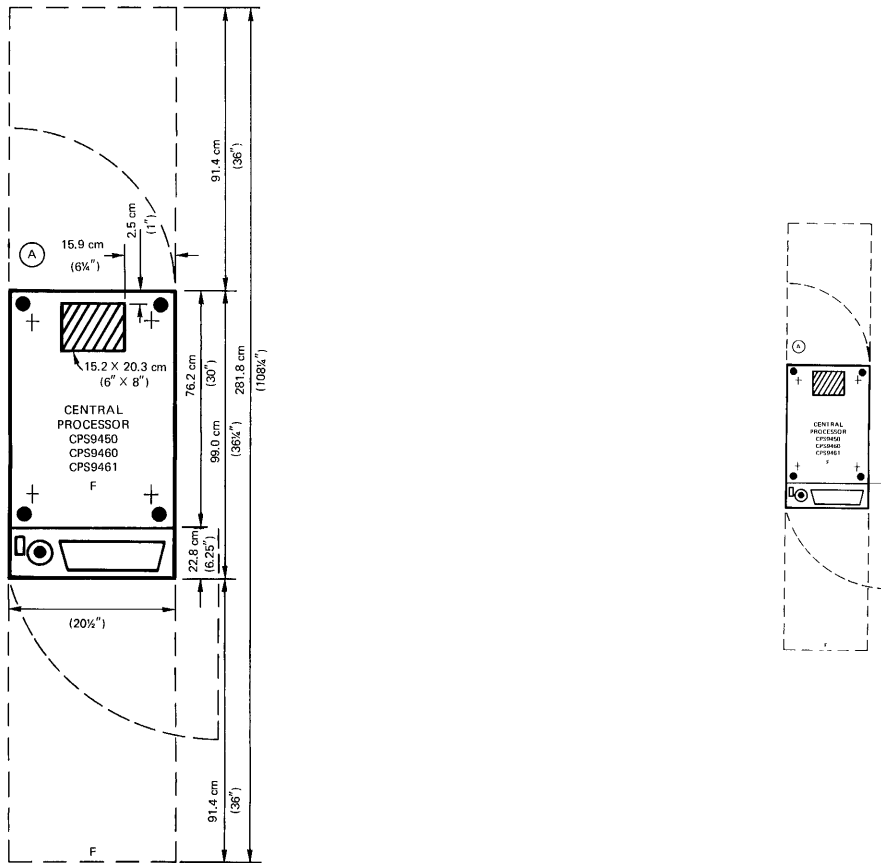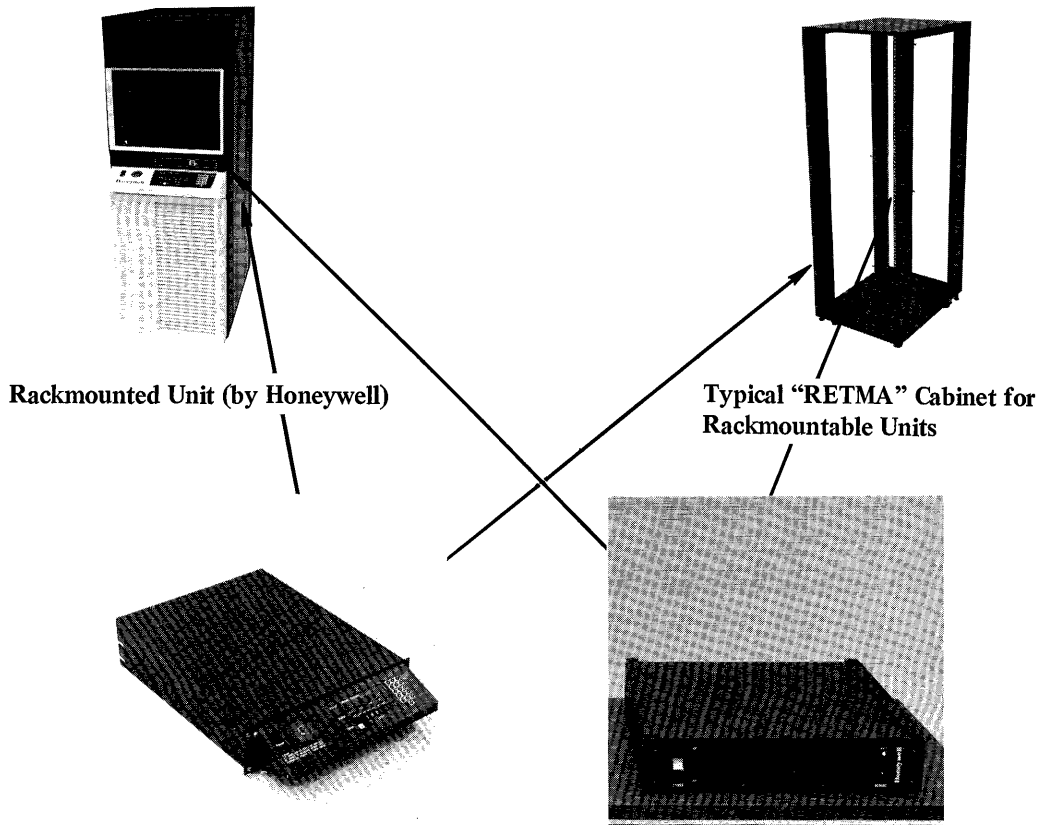
Figure 8-11 (cont). Typical Level 6 Layouts and Templates

Tabletop Central Processor
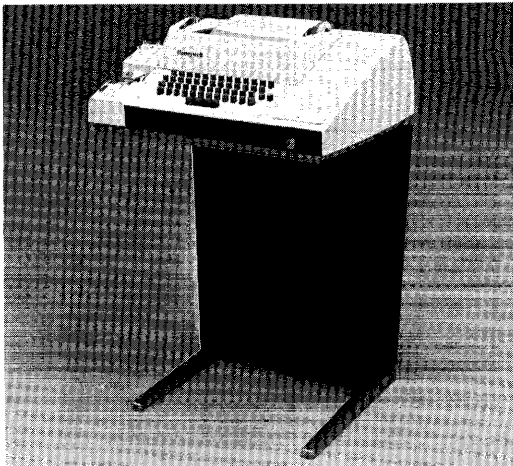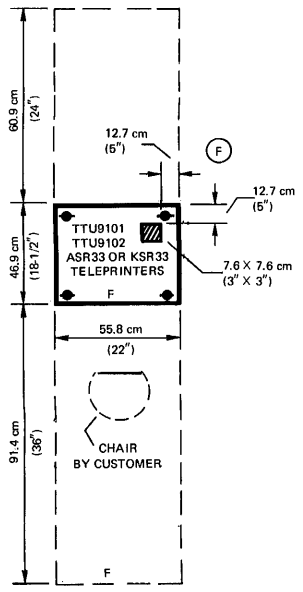
CENTRAL
PROCESSOR
CPU9450
CPU9460
CPU9461
(TABLETOP CAB9001)

F

12.7 cm
(5")

7.6 cm
(3")

91.4 cm
(36")

77.9 cm
(30-3/4")

50.5 cm
(19-7/8")

91.4 cm
(36")

ASR33 or KSR33 Teleprinter

TTU9101
TTU9102
ASR33 OR KSR33
TELEPRINTERS

F

60.9 cm
(24")

12.7 cm
(5")

12.7 cm
(5")

7.6 X 7.6 cm
(3" X 3")

46.9 cm
(18-1/2")

55.8 cm
(22")

91.4 cm
(36")

CHAIR
BY CUSTOMER
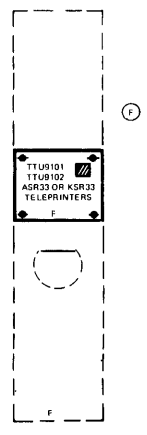
Figure 8-11 (cont). Typical Level 6 Layouts and Templates
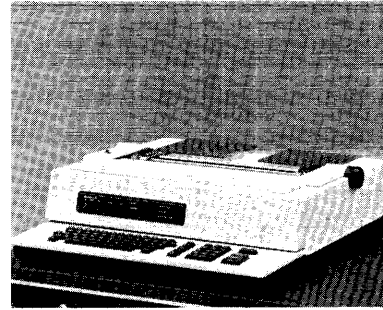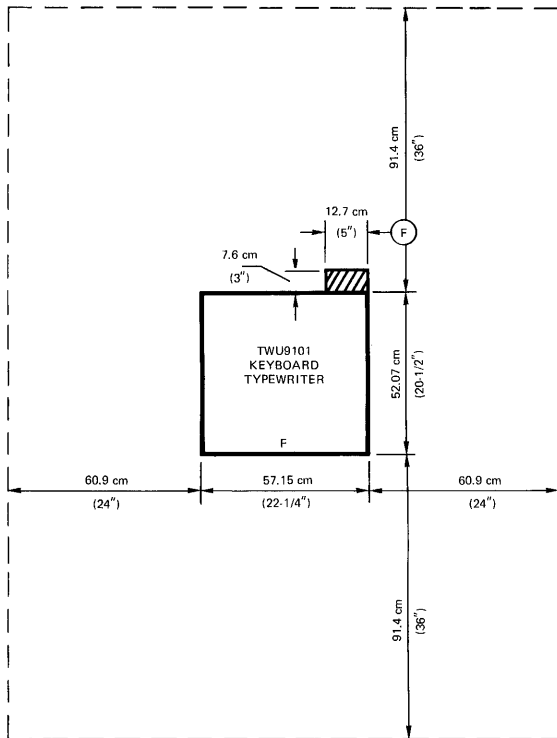
Tabletop KSR30 30 CPS Keyboard Typewriter Console
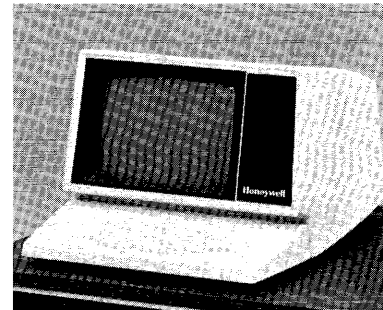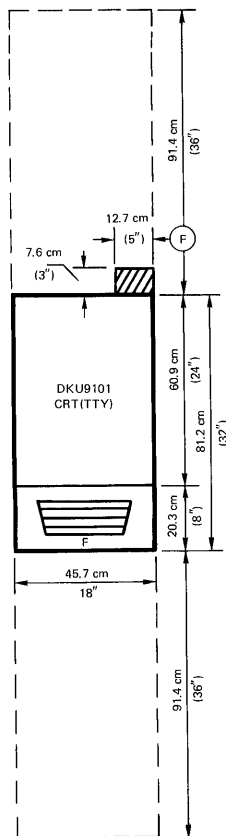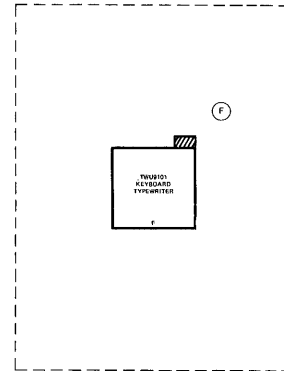
Tabletop CRT (TTY) and Keyboard
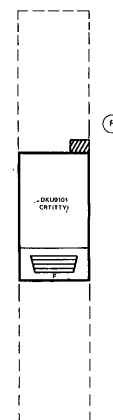
Figure 8-11 (cont). Typical Level 6 Layouts and Templates

Single or Dual Diskette Rackmounted Unit
(by Honeywell)

Single or Dual Rackmountable Unit
(by Customer)
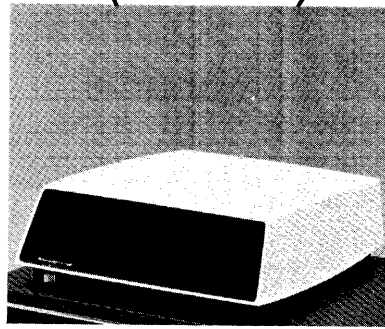
Tabletop Single or Dual Diskette

Figure 8-11 (cont). Typical Level 6 Layouts and Templates

Rackmounted (by Honeywell)
Cartridge Disk Units

Rackmountable (by Customer)
Cartridge Disk Units
Note:
Must be attached (plug into) Honeywell's PDU.
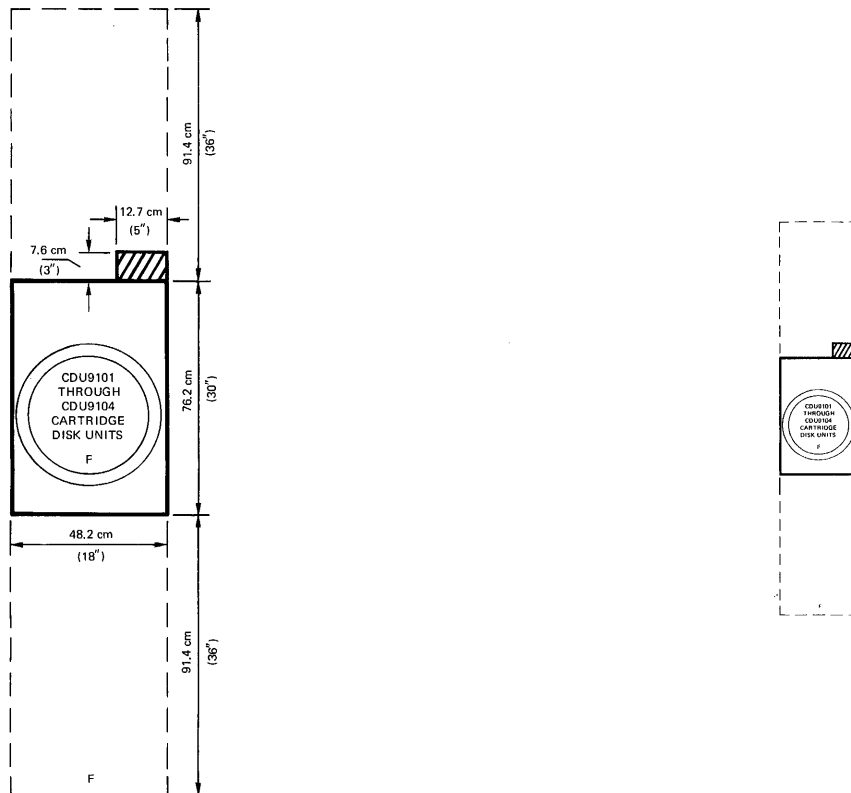
Figure 8-11 (cont). Typical Level 6 Layouts and Templates

Extension Table Wing Option (by Honeywell) Serial Printer

Pedestal Serial Printer (by Customer)
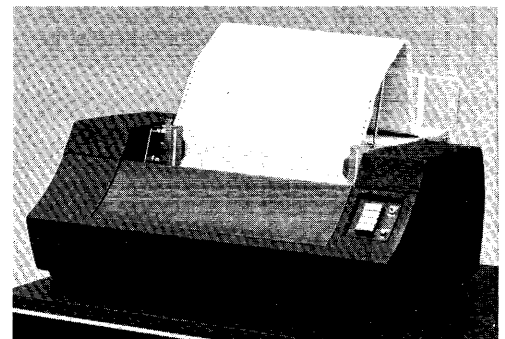
Tabletop Serial Printer
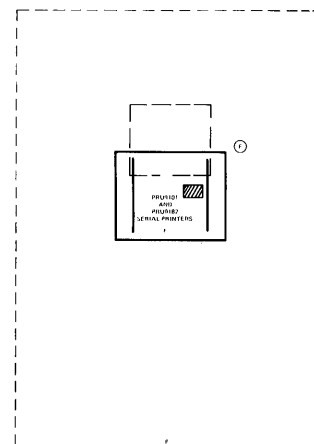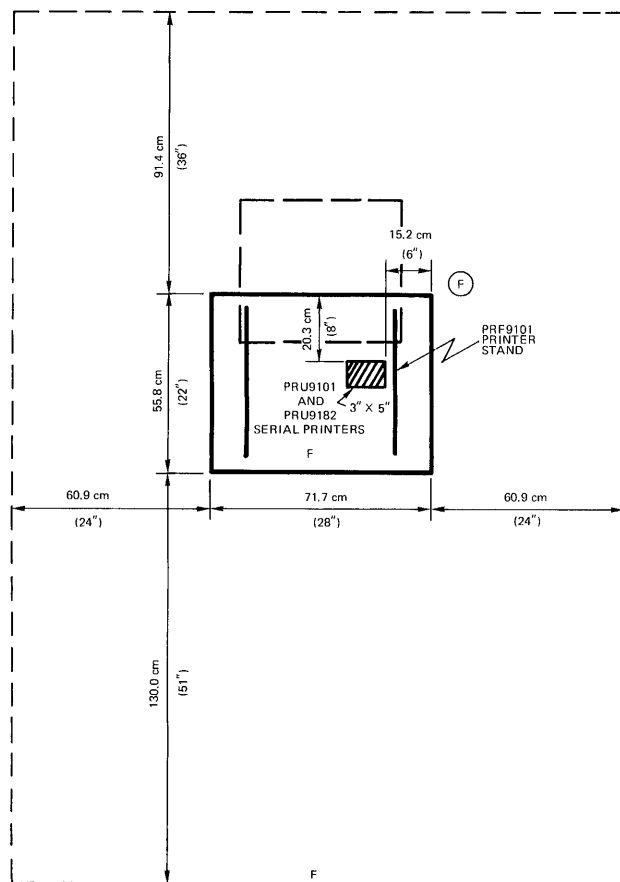
Figure 8-11 (cont). Typical Level 6 Layouts and Templates

Freestanding Line Printer
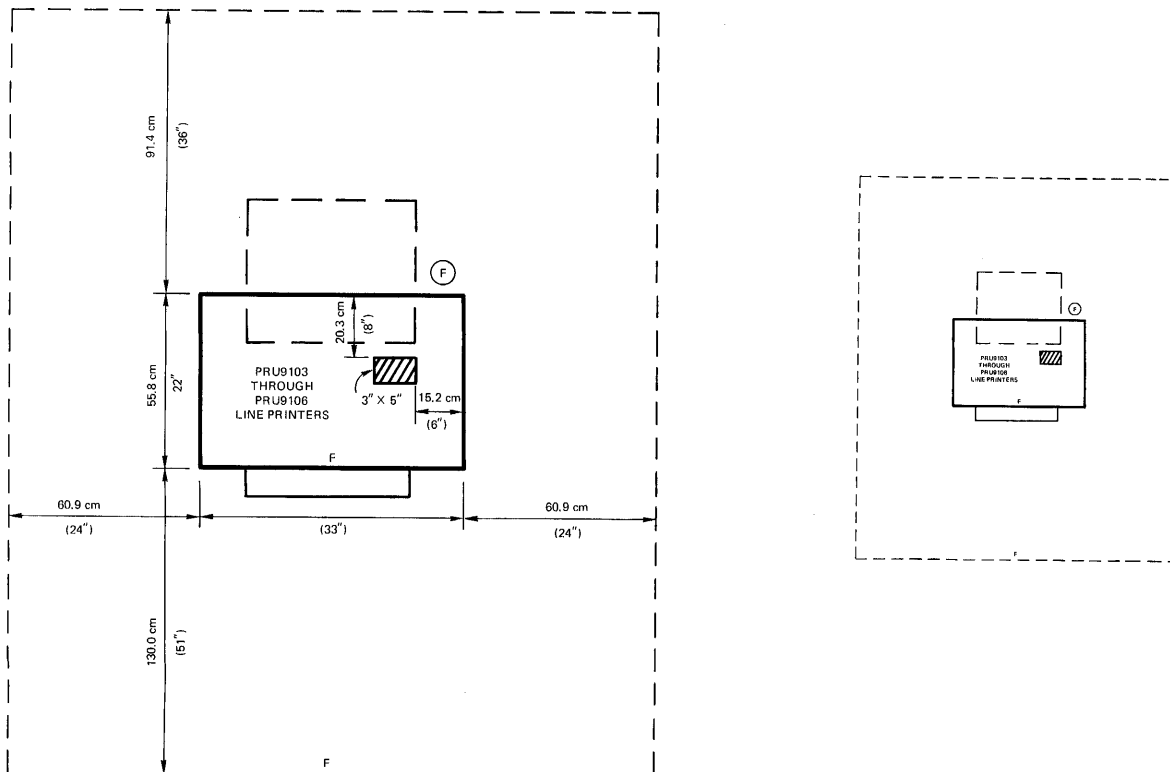
Figure 8-11 (cont). Typical Level 6 Layouts and Templates
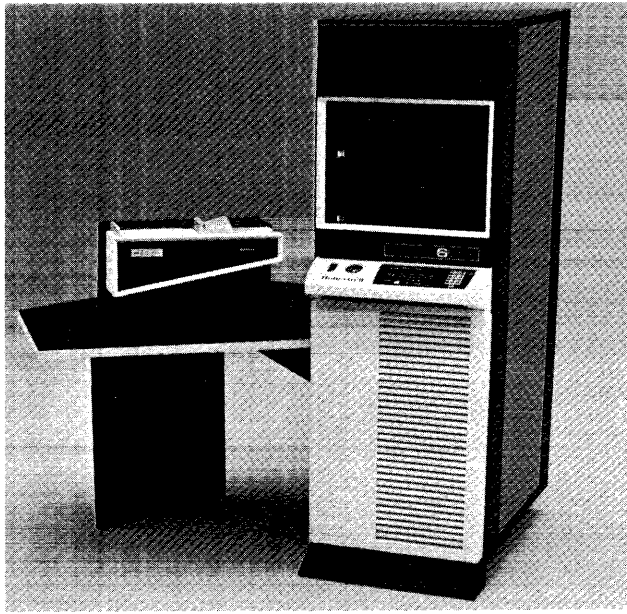
Extension Table Wing Option Card Reader (by Honeywell)
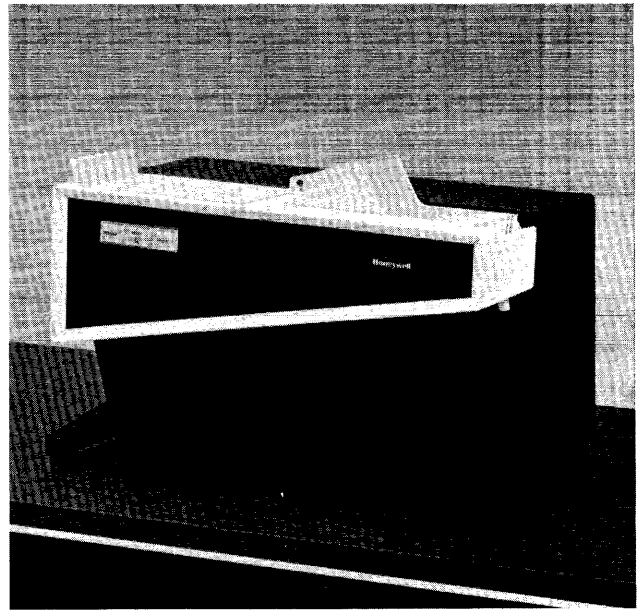
Tabletop Card Reader
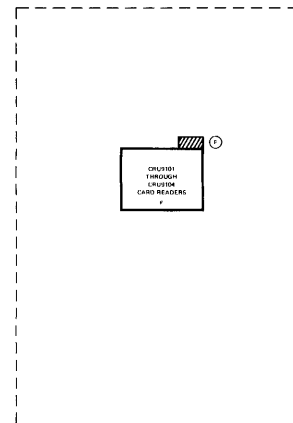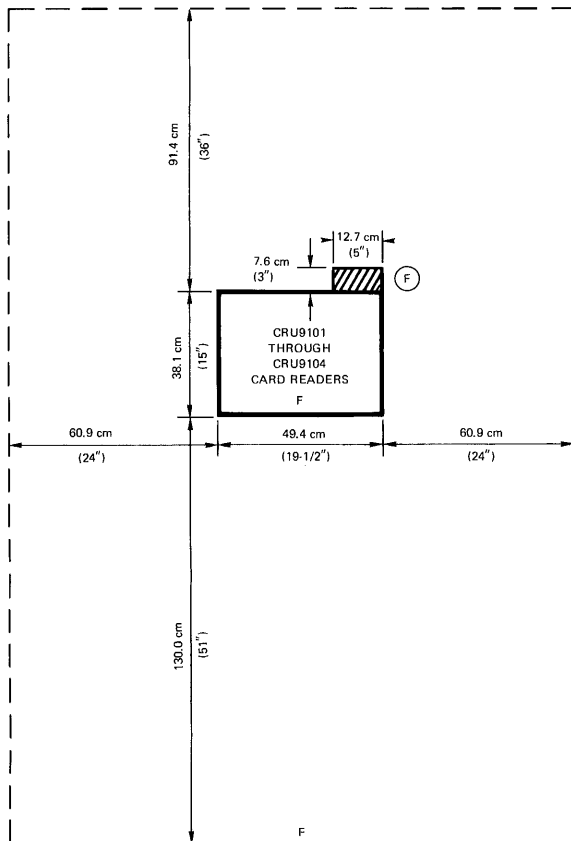
Figure 8-11 (cont). Typical Level 6 Layouts and Templates
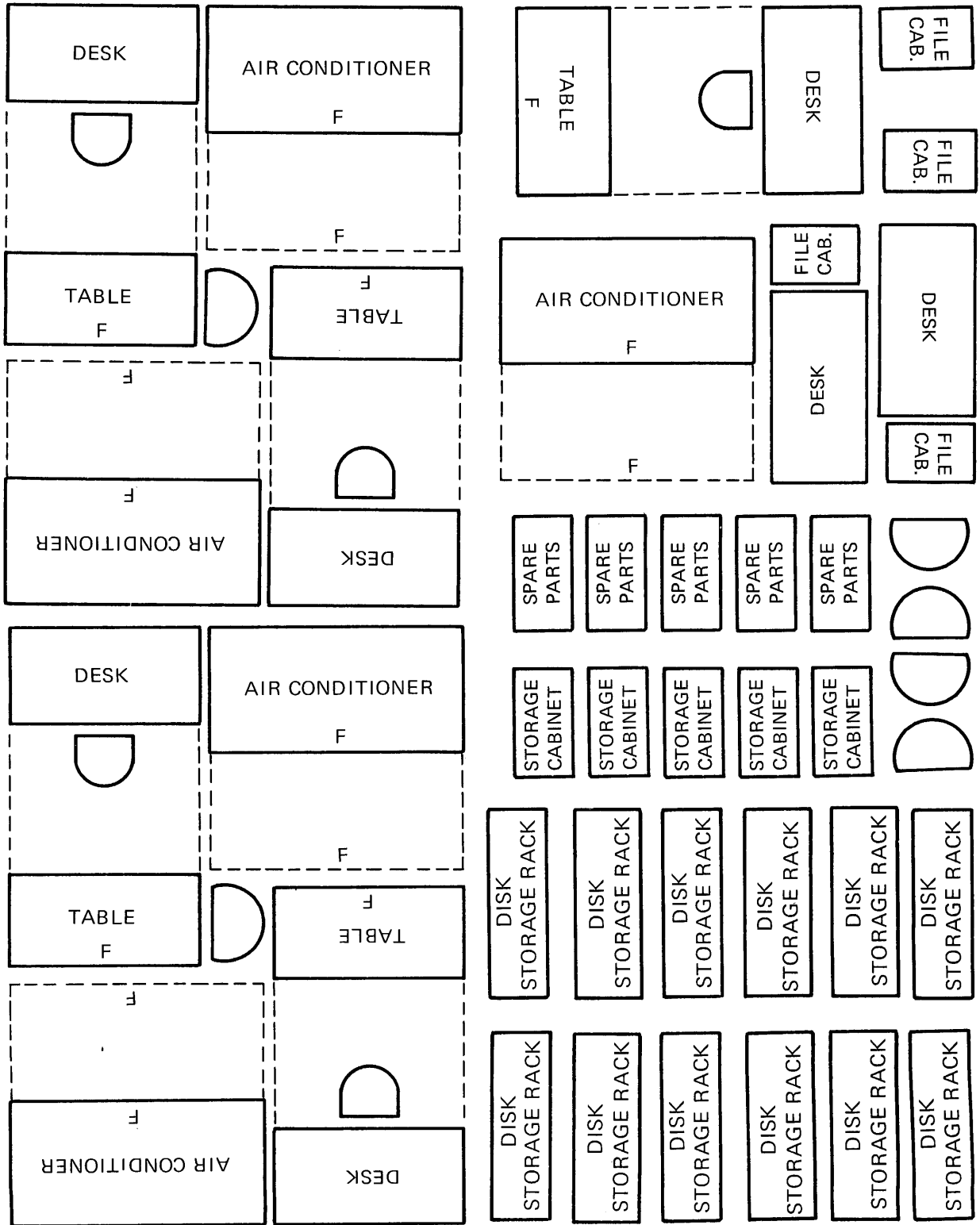
Figure 8-12. Layout Furniture Templates

–ELECTRICAL–

GENERAL:

A. Ac power will be supplied by the customer based on the requirements listed in these specifications.

B. The electrical power source will be independent and isolated from all other loads.

C. An allowance for expansion is recommended. (See Sheet 2 for specifications.)

D. All wiring must be installed in accordance with the National Electrical Code and other local ordinances. Costs for installing and/or modifying will be borne by the customer.

E. The electrical ground source shall be free of ground loops.

REQUIREMENTS:

A. The customer will supply and install in the computer room all AC receptacles indicated in the system layout and in Table 8-6 for individual unit specifications.

B. AC Power requirements for Level 6 Systems central processor cabinet and expansion cabinets (add-ons) (either of the following sources may be utilized):

    1. Input voltage should be from a 208 VAC RMS, 60 Hz, three-phase (one phase not used), 4-wire plus ground source with 24A at 208 VAC RMS, or

    2. 240 VAC RMA center-tapped (neutral 60 Hz, single-phased, 3-wire, plus ground source. If 240 is used, the Hubbell 25414 or 25403 (customer supplied) must be wired with the high lines ("hot" wires) connected to pins X & Y and the neutral center tap connected to pin W.

    3. Loading on the input lines will be from phase to neutral on two phases only. Maximum load current per phase will be 24A; there is no internal provision or procedure for balancing the load. The unused phase is truncated at the input connector. Cabinet containing central processor requires a drop; second cabinet (options) is slave to central processor cabinet. If third cabinet is required, another drop is used. Fourth cabinet, if required, is slaved to third. All cabinets requiring drops receive a "primary power contactor pick" voltage from central processor cabinet. No growth factor required.

C. Listed below are the electrical specifications for the Level 6 System peripherals.

    1. Load –   KVA for peripherals only.

    2. Voltage – 120/208 ± 10%, 3-Phase (only use two phases of the three phases).

    3. Frequency – 60 Hz ± 1/2 Hz

    4. Phase and number of wires as indicated.

    NOTE: The equipment neutral wire must not be connected to building ground except at power source (transformer, or building service entrance).

In the unusual cases wherein the power company does not regulate its power within the above tolerances and/or your facility imposes heavy loads on their substations, you are advised to furnish and install a voltage regulator.

Interconnecting cables between units shall be protected from mechanical injury. Product line raceways can be purchased through your Honeywell sales representative if raised flooring is not used. Raceway specifications are available from your Honeywell site planning engineer. The cost of supplying and installing raceway will be borne by the customer.

Figure 8-13. Installation Specification Format (Sheet 1)

Honeywell

—AIR CONDITIONING—

GENERAL:

A. The heat dissipation figures listed on Sheet 2 for each unit *do not include* the heat gain from other sources: namely, lighting, people, building transmission, and fresh air loads. The total, however, allows for a 30% growth in equipment and should be considered when figuring the size of the air-conditioning system.

B. Check NFPA-75 for fire protection information.

C. Costs for installing and/or modifying air-conditioning will be borne by the customer.

REQUIREMENTS:

A. Listed below are the air-conditioning specifications.

1. Cooling required for equipment only ____ kcal/hr or ____ watts (____ Btu/hr or ____ tons).

2. Temperature measured at input air of minisystem units — 23°C ± 3°C (73°F ± 5°F).

3. Relative humidity — 40 to 60%.

4. Filtration — Normal, unless environment is subjected to corrosive gases, salt air, or other unusual conditions, in which case special filtering will be required. If mechanical filters are used, their efficiency rating shall not be less than 20%.

5. It is strongly recommended that the computer room air-conditioning system be a separate system because computer rooms require year-round cooling. (Window-type air-conditioning units are not recommended.)

REFERENCES:

For additional information and recommendations concerning the above subjects, as well as acoustical ceilings, fire control, cables, etc., contact your local Sales Representative or Field Engineer.

Figure 8-13 (cont). Installation Specification Format (Sheet 2)

INITIAL CONFIGURATION — (Metric Measurements)

Qty.	Device	Marketing Identifier	Electrical Power		Receptacles (Symbol/type)	Heat Gain (kcal/hr or watts)	Weight (kg)	Dimensions W/D/H (cm)	Cables (m)	
			(kVA)	(amps)					ac	dc
		Total								
		30% Growth Factor								
		GRAND TOTAL								

Figure 8-13 (cont). Installation Specification Format (Sheet 3)

INITIAL CONFIGURATION — (Metric Measurements)

Qty.	Device	Marketing Identifier	Electrical Power		Receptacles (Symbol/type)	Heat Gain (kcal/hr or watts)	Weight (kg)	Dimensions W/D/H (cm)	Cables (m)	
			(kVA)	(amps)					ac	dc
Total										
30% Growth Factor										
GRAND TOTAL										

Figure 8-13 (cont). Installation Specification Format (Sheet 4)

LEGEND

+	Casters
●	Levelers
◆	Level and lock casters
F	Front of unit
-----	Clearance
▨	Unit cutout
▩	Power panel (by customer)
▬	Operators Extension Table Support
■	Control panel
▪	Legs and casters (casters are replaced by levelers)
⑮	Raceway callout
A Ⓐ F Ⓕ	Receptacle supplied and installed by customer (when specified)
By Customer Ⓛ	Power Plug Single Phase Straight Blade, U-ground, 5 Amp, 3-Wire, 125V

Figure 8-14. Floor Layout Grid
Scale: 1:50mm (1/4 in.)

APPENDIX A

SITE FACILITIES LISTING

SITE FACILITIES LISTING

Outlined below is a site facilities check-off list that should be considered before you select or plan your computer site.

Space Requirements

- Service Engineering Area
  Based on system size or area should be planned for test equipment, manuals, and parts necessary for system checkout and maintenance.
- Media Storage Facilities
  Again based on size of your installation, space must be allotted for storage of disk packs, printer paper and ribbons, cards, and other supplies.

Equipment Structural Tolerances

Although Honeywell equipment can withstand intermittent building vibrations or minor Richter Scale shocks, Honeywell does not guarantee a design vibration tolerance that might be experienced at your particular site. If vibrations and shock are apparent at your location, they should be measured and discussed with your engineering consultant.

Floor

- Loading
  Model 6/34 and 6/36 equipment units do not impose structural modification in existing buildings having a normal line loading capacity of 244 kg/sq m (50 lb/sq ft.).
- Pitch
  Check local building codes for degree-of-pitch requirements. A 2.79 cm (1.10″) slop ratio generally is acceptable.
- Surface Metal Raceway
  Each device in the configuration has control and signal cables that must be protected. Surface metal raceway, or "trough" is an economical enclosure for wires and cabling.

(Cable protection within the devices is included in the equipment design.) Honeywell has raceway available for Level 6 systems. (See Honeywell *Computer Supplies Cataloge*, Order No. BY62, or your Honeywell Marketing Representative.)

- Floor Covering
  Many considerations besides appearance and cost determine the best floor covering material for a minicomputer installation.

  Tile – In the past, the choice of hard surface flooring has usually narrowed down to vinyl or linoleum materials because of their attractiveness, durability, maintainability and sound absorption.

  Carpet – Carpeted floors offer many advantages over tile floors. A good grade of carpet, however, lasts as long as good vinyl tile, and can be treated to be lint free and without static electricity.
- Maintenance
  The beginning of a good maintenance program is prevention: place track rugs at all entrances to catch dust, grit and abrasives brought in from other areas.

  Walls – All installation walls must be from floor to ceiling, to avoid noise in the area and minimize dust filtration.

  Ceilings – Any commercial grade of fire-resistant ceiling tile serves adequately and produces an attractive, clean appearance.
- Soundproofing
  A minicomputer system does have a higher noise level than a clerical office containing light office machinery. Therefore, keep the noise in the system area – and nearby – at an acceptable level, pay particular attention to the use of sound-absorbing materials and to the arrangement of sound barriers.
- Lighting
  An intensity of approximately 371-743 lux (40-80 foot candles) at desk level is adequate for the minicomputer area.

Air Conditioning
- Monitoring Temperature and Humidity
  Continuous monitoring of the site's temperature and humidity is recommended as a way to save downtime. Recording instruments will indicate, for example, the extent and duration of any undesirable environmental conditions.
- Air Filtration
  Air filtration is an essential adjunct to the regular cleaning regime to help ensure con-

tinuous and reliable operation of Disk devices.

Mechanical Air Filters – High-efficiency air filters are satisfactory unless the installation is subjected to corrosive gases, salt air, or other unusual conditions.

Electronic Air Cleaners – Electronic air cleaners are highly recommended where clean air is a major problem. Honeywell's Residential Division is a supplier and can be contacted for sales or service via

> Honeywell Inc.
> Honeywell Plaza
> Minneapolis, MN 55408

- Types of Systems
  There are four types of systems Honeywell recommends:
  Overhead Supply
  Underfloor Supply
  Combination Supply
  Freestanding Supply

Electrical Power
- Power Distribution
  If the electrical power at the installation is not of the required voltage, one or more transformers must be purchased and installed. The capacity required depends upon the equipment complement and what is specified in the calculated installation specification.

  Wye – The wye connected distribution transformer is the way the required three-phase, 120/208 voltage source can be obtained. You may already have this voltage supplying the site, since the wye is widely used in urban areas.

  Delta – The delta method of power distribution is probably the next most popular way to distribute power. The common delta is a four-wire system comprising three phase and neutral such that the voltage between any two phases is normally 240 volts.

  Open Delta – To save the cost of a transformer, an open delta system is sometimes used. This system develops the same voltage as the closed delta.
- Transformers
  Transformer(s) can be general purpose, isolated, dry type, cooled by air convection, and suitable for indoor service in either a wall mounted or floor-mounted position.
- Isolated Transformers
  Level 6 system must be protected by an isolation transformer.

- Voltage Regulators
  A suitable voltage regulator is an automatic, dry type, cooled by air convection, and complete with enclosure for indoor service.
- Phase Rotation
  The three-phase and single-phase power receptacles and/or connectors used in conjunction with a device's male plug must be wired correctly. Correct phase rotation is an important safety measure for wiring all devices.

  Earth Grounds – An earth ground is a network of parts such as ground plates, rods, mats, radials, or cables that provides a low-impedance conducting path between a facility and the absolute earth. The design objective should be to have the resistance to ground as near to zero as possible.

  "Green Wire" Safety Ground – Every subsystem power run must have a separate, continuous, insulated wire for use as a frame (protective) ground referred to as "the green wire." It is run inside the conduit or power cord with the conductors and ac neutral. The frame ground wire must be securely fastened to the frame ground bus or terminal provided in the equipment and to the power distribution panel frame or ground bus (not the ac neutral bus).

COMMUNICATIONS FACILITIES

The integrated communications controller attaches directly to the Level 6 integrated unit processor via a device adapter interface. The communications controller uses the extensive I/O and microprogramming capabilities of its own to expand its processing power and form the nucleus of the communications handling facility.

- Terminals
  Your Honeywell Marketing Representative has information about terminals compatible with our communication interfaces. The type and quantity of terminals (communication modems, phone lines, etc.) must be decided two or three months before system delivery to ensure that the terminals will be delivered and installed before the mini computer system arrives.
- Power
  The local telephone company can make provisions for the required communications devices. In some cases the telephone company also provides multiplexers. Since all such units require 115 Vac outlets, consult with the telephone representative to deter-

mine the correct number of outlets and locations.

Safety is a vital factor for a processing center. Safety should be a consideration in the choice of a location, building materials used, fire prevention, equipment, and personnel training. Your mini computer room should be a noncombustible or fire-resistant building or area.

- Fire Protection

Fire prevention is an important installation requirement. Protection is greatest when the computer is housed in a fire-resistant building. The ceiling, floor and walls of the computer room should be of noncombustible material. The room may be separated from adjoining areas by double fire doors. An automatic fire and smoke detection system should be considered. The air conditioning system should be provided with fire dampers and its ducts should be independent of all other ducts in the building.

Extinguishers — At least two carbon dioxide fire extinguishers should be present in each room where computer equipment is located. If a sprinkler system is used, some precaution should be taken against accidental discharge of water. It is recommended that a copy of Protection of Electronic Computer Systems (NFPA No. 75)[a] be thoroughly reviewed.

Monitoring Systems — Honeywell's Commercial Division offers data processing customers a wide array of protective systems that can be installed individually or integrated into a complete monitoring system not only for fire and smoke, but also other building facility needs such as environmental automation, waterflow detection, security, sprinkler supervision, elevator control, equipment monitoring and many other protective systems. For information about protective systems, consult your local Honeywell Commercial Division Office or:

> Honeywell
> Honeywell Plaza
> 2701 Fourth Avenue South
> Minneapolis, MN 55408

- Lightning Protection

Primary power transformers must be protected by lightning arrestors. It is highly desirable that similar protection be provided at the service entrance to the building.

Arrestors reduce the possibility that excessive voltage and currents due to lightning strikes will seek some indeterminate, low-impedance path to ground, such as building metallic structure or equipment cabinets.

- Emergency Power-Off Wiring

The National Electrical Code-1968 requires each exit from the computer room be equipped with a control system and air conditioning equipment, to be used in an emergency. In large installations, fire alarms, controls, and control pull boxes are also to be located at each exit and the fire alarm circuit integrated with the emergency-off circuit.

- Emergency Lighting

Some local codes require a special battery-operated lighting unit that automatically illuminates an area in case of power or lighting circuit failure.

- Security

Do not overlook the serious matter of computer area security. At the very least, extend the existing building security systems and services to include the minicomputer area.

MEDIA STORAGE AREA

A storage area for disk packs, punched cards, printer paper, spare parts, and manuals should be provided. These items should be housed in metal containers or fire-resistant cabinets. For the most efficient operation, the storage area should be located in or adjacent to the minicomputer.

- Disk Packs

Disk packs must not be exposed to intense heat and should never be stored in direct sunlight or stacked on top of other packs. The storage area temperature should range from 10°C -32°C (50°F090°F), with a relative humidity range between 10% and 80%, provided a wet bulb temperature reading never exceeds 29°C (85°F).

- Cards and Printer Paper

Cartons of cards should be stacked upright to prevent warping or bending. Cards should not be placed directly on the floor, but should be squared neatly and stored in a dust-free container, preferably in a card filing drawer. Do not use elastic bands in bundling card decks.

Paper products should not be stored where they are exposed to variations in temperature and humidity, such as near heated pipes, radiators, windows, or air ducts.

SHIPPING AND MOVING IN

- Shipping
  Honeywell makes all the necessary arrangements for shipping and insuring the computer system and components. Honeywell has the responsibility of keeping you aware of the selected delivery dates and approximate costs. Special arrangements can be made before shipment, with the approval of Honeywell.
- Moving In
  Moving expenses vary, depending on the ease of access to the installation site. Existing corridors (including turns), doorways, and elevator shafts should be large enough to accommodate the following dimensions:

  - Width — 0.91m (3 ft.)
  - Depth — 1.22m (4 ft.) (on floor, not including saddles, sills, etc.)
  - Height — 2.13m (7 ft.) (includes height of shipping dolly)

Elevators should be capable of carrying at least 900 kg (2000 lb). Saddles and sills should be omitted to permit unhindered movement of the unit through doorways.

If any of the above mentioned presents a problem the Honeywell Marketing Representative should be informed of the problem. In this way Honeywell can make special arrangements for mover/trucking firms to deliver equipment without unforeseen delay to the computer room.

APPENDIX B

INSTRUCTION TIMINGS

This section provides the following timing tables:

- Instruction and Operand Fetch Times
  (Table B-1)
- Execution Times
  (Table B-2)
- Shift and Generic Instruction Times
  (Table B-3)
- R-Branch, I-Branch Execution Times
  (Table B-4)
- I/O Instruction Times
  (Table B-5)

TABLE B-1. INSTRUCTION AND OPERAND FETCH TIMES

Opcodes/Fetch Times (μs)

Addressing Forms	LDB, SWB, CMB, LDR, SWR, CMR, ADD, SUB, MUL, DIV, OR, XOR, AND, INC, DEC, CAD, CMZ, CPL, NEG, LEV, MTM	STB, STR, STM, CL, SAVE, JMP, RSTR, LNJ, ENT, LAB	LDH, LLH, CMH, ORH, XOH, ANH		STH, CLH	LB, LBF, LBC, LBS, LBT	LDV, CMV, ADV, MLV
			+ Operand	– Operand			
IMA, P + D, B + D[a]	3.72	2.77	4.01	3.72	2.77	3.72	Total Fetch and Execution times for immediate operands are shown in Table B-2.
IMA + X[a]	4.01	3.06	4.59	4.30	3.35	5.17	
B[a], IMO	2.77	1.82	3.06	2.77	1.82	2.77	
B + X[a]	3.06	2.11	3.64	3.35	2.40	4.22	
↓B, B↑	3.06	2.11	3.35	3.06	2.11	3.06	
B + ↓X, B + X↑	3.35	2.40	3.93	3.64	2.69	4.51	
R Register	1.53	1.53	2.49	2.21	1.53	1.53	
B Register	1.53	1.53	–	–	–	–	

[a]If indirect add 1.24 μs to time shown.

TABLE B-2. EXECUTION TIMES

Op Codes	Address Syllable Times (μs)	
	R Register B Register	Any Other
INC, DEC, NEG, CPL, CL, STR, STB, STS	0.58	1.16
CLH, STH	1.16	1.16
STM	0.87	1.45
SWR, SWB	1.16	1.74
CAD	0.58/0.87	0.58/1.45
LBS (I[B] = 1), LBT	1.16	1.74/3.07
LBS (I[B] = 0), LBF, LBC	1.45	2.03/3.36
JMP, ENT	—	0.58
LNJ	—	0.29
LAB	—	0.0
ADD, SUB	0.38	
LDR, LBD, LDH, OR, XOR, AND, ORH, XOH, ANH	0.29	
CMR, CMB, CMH	0.38/0.67	
CMV[a]	1.91/2.20	
CMZ	0.67/0.96	
LEV	4.60/88.20	
SAVE	13.21/22.71	
RSTR	12.63/34.30	
MTM	1.74	
MUL (# ≠7)	11.20	
MUL (# =7)	10.73	
MLV[a] (# ≠7)	12.73	
MLV[a] (# =7)	12.26	
DIV (# ≠7)	13.22/14.56	
DIV (# =7)	13.22/14.27	
LLH	0.58	
LB	0.87	
ADV[a]	1.91	
LDV[a]	1.82	
CMN		
LDI		
SDI	To be supplied	
SRM		
IOH		
LEV		

[a]Total Fetch & Execution Time

TABLE B-3. SHIFT AND GENERIC INSTRUCTION TIMES (INCLUDES FETCH)

Shift Instruction Times (μs)		
SOL	1.53 + 0.29d	
SAL	1.82/2.11 + 0.29d	
SCL	1.53 + 0.29d	
DCL	1.82 + 0.29d	
DOL < 16	1.82 + 0.29d	(See Notes a and b)
DOL ⩾ 16	2.11 + 0.29d	
DAL < 16	1.82/2.11 + 0.29d	
DAL ⩾ 16	2.11/2.69 + 0.29d	
SOR	1.53 + 0.29d	
SAR	1.53 + 0.29d	
SCR	1.53 + 0.29d	
DCR	1.82 + 0.29d	
DOR < 16	1.82 + 0.29d	
DOR ⩾ 16	2.11 + 0.29d	
DAR < 16	1.82 + 0.29d	
DAR ⩾ 16	2.11 + 0.29d	
Generic Instruction Times (μs)		
HLT	2.11	
MCL, BRK	16.75/17.07	
RTT	11.85	
RTCN, RTCF	2.11	
WDTN, WDTF	2.11	

NOTES: [a] d = shift distance; 0 ⩽ d ⩽ 15

[b] These are times for procedural shifts. For nonprocedural shifts (d = 0) add: 0.96 μs to the above times.

TABLE B-4. R-BRANCH, I-BRANCH EXECUTION TIMES (INCLUDES FETCH)

Op Code / Test Success and Addressing Mode	Unsuccessful (μs)	Successful (μs)		
		$d \neq 0, 1$ (P + d)	d = 0 (IMA)	d = 1 (P + D)
BLZ, BGEZ, BEZ, BNEZ, BGZ, BLEZ, BEVN, BODD, BINC, BDEC, BOV, BNOV	1.82	2.40/2.69 min/max	3.35	3.35
B, NOP, BAL, BAGE, BE, BNE, BAG, BALE, BL, BGE, BG, BLE, BSU, BSE, BCT, BCF, BBT, BBF, BIOT, BIOF	1.53	2.11/2.40	3.06	3.06

NOTE: If indirect (*IMA, *B + X, etc.), add 1.24 μs to time shown.

TABLE B-5. I/O INSTRUCTION TIMES

Address Syllable Form	I/O Instruction Times (μs)		
	IO		IOLD
	Input	Output	
IMA[a], P + D[a], B + D[a]	10.60	10.94	15.18
IMA + X[a]	11.18	11.52	16.34
B[a], IMO	8.70	9.04	12.33
B + X[a]	9.28	9.62	13.49
↓B, B↑	9.28	9.62	13.20
B + ↓X, B + X↑	9.86	10.20	14.36
IV + D	13.66	14.00	19.77
RA	6.22	5.93	8.32

[a]If indirect in any address syllable, add 1.24 μs for each indirection.

HONEYWELL INFORMATION SYSTEMS
Technical Publications Remarks Form

TITLE	SERIES 60 (LEVEL 6) LEVEL 6 MINICOMPUTER HANDBOOK	ORDER NO.	AS22, REV. 0
		DATED	JANUARY 1976

ERRORS IN PUBLICATION

SUGGESTIONS FOR IMPROVEMENT TO PUBLICATION

Your comments will be promptly investigated by appropriate technical personnel and action will be taken ☐
as required. If you require a written reply, check here and furnish complete mailing address below. ☐

FROM: NAME _____   DATE _____

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Honeywell

CUT ALONG LINE

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AS22, Rev. 0

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SERIES 60 (LEVEL 6)

HARDWARE

SUBJECT:

Additions and Changes

SPECIAL INSTRUCTIONS:

This is the first addendum to AS22, Rev. 0, dated January 1976.

Insert attached pages into the manual according to the collating instructions on the back of this cover. Change bars in the margins indicate technical additions and changes; asterisks denote deletions. These changes and additions will be incorporated into the next revision of the manual.

NOTE: Insert this manual cover after the manual cover to indicate the updating of the document with Addendum A.

DATE:

October 1976

ORDER NUMBER:

AS22A, Rev. 0

COLLATING INSTRUCTIONS

To update the manual, remove old pages and insert new pages as follows:

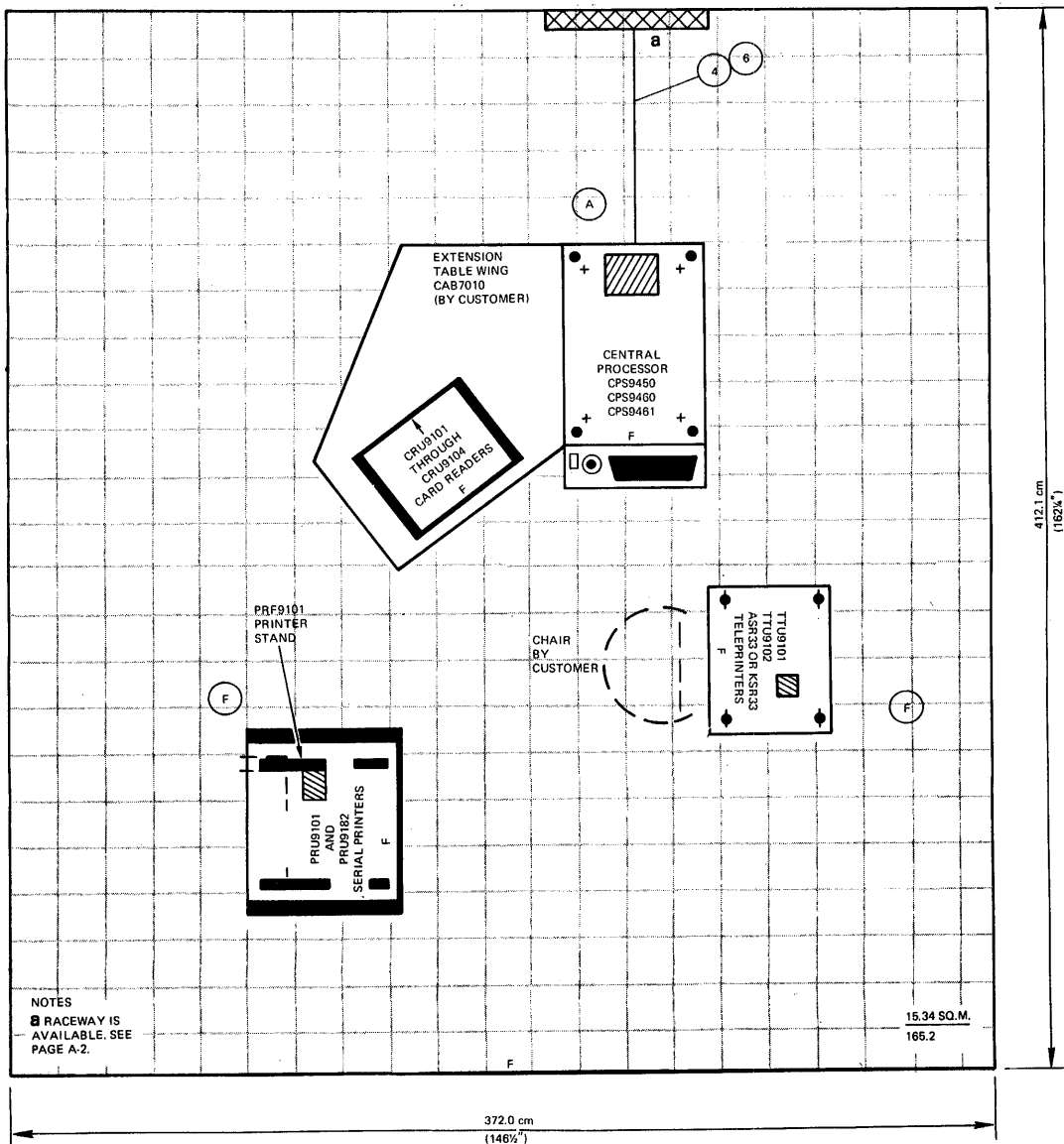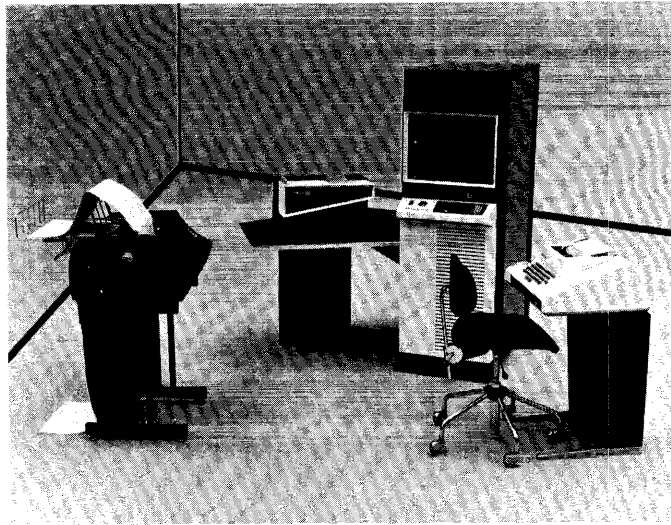| Remove	Insert
v and vi	v and vi
8-11	8-11
8-12	8-12
8-13	8-13
8-14	8-14
8-15	8-15
8-16	8-16
8-17	8-17
8-18	8-18
	8-18.1
8-19	8-19
8-20	8-20
8-21	8-21
8-22	8-22
8-23	8-23
8-24	8-24
8-47	8-47
8-49	8-49
8-51	8-51
8-53	8-53
8-55	8-55

ILLUSTRATIONS

Figure 8-5. Typical System Layout Requirements

– TYPICAL SYSTEM ELECTRICAL REQUIREMENTS –

GENERAL:

A. Ac power and electrical ground source will be supplied by the customer based on the requirements listed in these specifications.

B. The electrical power source should be independent and isolated from all other loads, where applicable.

C. An allowance for expansion is recommended. (See Sheet 2 for specifications.)

D. All wiring must be installed in accordance with the National Electrical Code and other local ordinances. Costs for installing and/or modifying will be borne by the customer.

REQUIREMENTS:

A. The customer will supply and install all ac receptacles indicated in the system layout and in Table 8-6 for individual unit specifications.

B. Ac power requirements for Level 6 Systems central processor cabinet with power distribution unit (PDU) and expansion cabinets (add-ons). Any of the following sources may be utilized:

   1. Input voltage could be from a 208 VAC RMS, 60 Hz, two-phase, 3-wire, plus ground source with 24A at 208 VAC RMS, or

   2. 230/240/250 VAC RMS center-tapped (neutral) 60 Hz, single-phased, 3-wire, plus ground source. In either case, the Hubbell 25414 or 25403 (customer supplied) must be wired with the high lines ("hot" wires) connected to pins X and Y and the neutral center tap connected to pin W.

   3. Loading on the input lines will be from phase to neutral on two phases only. Maximum load current per phase will be 24A; there is no internal provision or procedure for balancing the load. The unused phase when three phase is used, is truncated at the input to the RF1 filter in the PDU. Cabinet containing central processor requires a drop; second cabinet (options) is slave to central processor cabinet. If third cabinet is required, another drop and PDU are used. Fourth cabinet, if required, is slaved to third. All cabinets requiring drops receive a "primary power contactor pick" voltage from central processor cabinet. No growth factor is required.

C. Listed below are the electrical specifications for the Level 6 System and devices:

Central Processor Cabinet and ASR33 Teletypewriter

Load – 12.08 kVA

Voltage – 120/208 ±10%

Frequency – 60 Hz ±1/2 Hz

Phase and number of wires as indicated.

PRU9101/9102 Serial Printer

Load – 0.85 kVA

Voltage – $120^{+10\%}_{-15\%}$

Frequency – 60 Hz ±1/2 Hz

Phase and number of wires as indicated.

NOTE: The equipment neutral wire must not be connected to building ground except at power source (transformer, or building service entrance).

In the unusual cases in which the power company does not regulate its power within the above tolerances and/or your facility imposes heavy loads on their substations, you are advised to furnish and install a voltage regulator.

Interconnecting cables between units shall be protected from mechanical injury. Product line raceways can be purchased through your Honeywell sales representative if raised flooring is not used. Raceway specifications are available from your Honeywell Sales Representative. The cost of supplying and installing raceway will be borne by the customer.

Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 1)

Honeywell

– TYPICAL SYSTEM ENVIRONMENTAL REQUIREMENTS –

GENERAL:

A. The heat dissipation figures listed on Sheet 2 for each unit *do not include* the heat gain from other sources: namely, lighting, people, building transmission, and fresh air loads. The total, however, allows for a 30% growth in equipment and should be considered when figuring the size of the air conditioning system.

B. Check NFPA-75 for fire protection information.

C. Costs for installing and/or modifying air conditioning will be borne by the customer.

REQUIREMENTS:

A. Listed below are the environmental specifications.

1. Cooling required for equipment only 3.385 kcal/hr or 3.933 watts (13435 Btu/hr or 1.1 tons).

2. Temperature measured at input air of minisystem units – 24°C ±-8.4°C (75°F ±15°F).
   Rate of change/hr – ±-5.6°C (10°F/hr). (No condensation.)

3. Relative humidity – 30 to 60%

4. Filtration – Normal, unless environment is subjected to corrosive gases, salt air, or other unusual conditions, in which case special filtering will be required. If mechanical filters are used, their efficiency rating shall not be less than 20%.

5. It is strongly recommended that any required air conditioning system be a separate system because year-round cooling is required. (Window-type air conditioning units are not recommended.)

REFERENCES:

For additional information and recommendations concerning the above subjects, as well as acoustical ceilings, fire control, cables, etc., contact your local Honeywell Sales Representative or Field Engineer.

Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 2)

Qty.	Device	Marketing Identifier	Electrical Power (kVA)	Receptacles (amps, symbol, type)			Heat Gain (kcal/hr or watts)	Weight (kg)	Dimensions W/D/H (cm)	Cables (m)	
										ac	dc
1	Central Processor System: Cabinet #1 CP - 64K PDU	CPS9460 CAB9003	Electrical Notes: A & B 8.64	1/30	Ⓐ	A	2016 2343	226.0	52.0/76.2/156.2 Control Panel Overhang	1.8	15.2
1	Extension-Table Wing	CAB9010	—	—	—	—	—	29.9	xxx/92.2/xxx		
1	Control Panel	————	within above cabinet					—	—	—	—
1	Memory Save and Autorestart	PSS9110	within above cabinet					—	—	—	—
2	Double Diskette	DIU9102	within above cabinet					—	—	—	—
1	Cartridge Disk Unit	CDU9101	within above cabinet					. .	—	—	—
1	ASR33 Teleprinter	TTU9101	within above cabinet				94 / 109	25.4	55.8/46.9/66.0	1.8	7.6
1	Serial Printer	PRU9101	0.45	1/15	Ⓕ	F	340 / 395	54.4	71.1/55.8/34.2	2.4	15.2
1	Serial Printer Pedestal	PRF9101	—	—	—	—	—	23.6	71.1/55.8/66	—	—
1	Card Reader	CRU9101	0.21	1/15	Ⓕ	F	154 / 179	15.8	49.5/38.1/34.2	1.8	15.2
	Total		9.30	—	—	—	2604 / 3026	375.1	—	—	—
	30% Growth Factor		2.79	—	—	—	781 / 907	112.5	—	—	—
	GRAND TOTAL		12.09	—	—	—	3385 / 3933	487.6	—	—	—

Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 3)

Qty.	Device	Marketing Identifier	Electrical Power (kVA)	Receptacles (amps, symbol, type)			Heat Gain (Btu/hr)	Weight (lbs)	Dimensions W/D/H (in)	Cables (ft) ac	Cables (ft) dc
1	Central Processor System: Cabinet #1	CPS9460	Electrical Notes: A & B 8.64	1/30	Ⓐ	A	(8000)	500	20½/30/61½ Control Panel Overhang xxx/36¼/xxx	6	50
	CP - 64K PDU	CAB9003									
1	Extension-Table Wing	CAB9010	–	–	–		–	66	24/30/30	–	–
1	Control Panel	———	within above cabinet					–	–	–	
1	Memory Save and Autorestart	PSS9110	within above cabinet					–	–		
2	Double Diskette	DIU9102	within above cabinet					–	–	–	
1	Cartridge Disk Unit	CDU9101	within above cabinet						–		
1	ASR33 Teleprinter	TTU9101	within above cabinet				(375)	56	22/18½/26	6	25
1	Serial Printer	PRU9101	0.45	1/15	Ⓕ	F	(1350)	120	28/22/13½	8	50
1	Serial Printer Pedestal	PRF9101	–	–	–	–	–	52	28/22/26	–	–
1	Card Reader	CRU9101	0.21	1/15	Ⓕ	F	(610)	35	19½/15/13½	6	50
Total			9.30	–	–	–	10335	82.9	–	–	–
30% Growth Factor			2.79	–	–	–	3100	24.8	–	–	–
GRAND TOTAL			12.09	–	–	–	13435	10.87	–	–	–

Figure 8-5. (Cont.) Installation Specifications and
Equipment Calculation Format (Sheet 4)

SPECIFICATIONS

The location of the minicomputer facility should be selected with regard not only for the decor space, clearance, operation of the minicomputer and its peripherals, but also for air conditioning, and electrical power. These considerations apply equally to new and old buildings.

Decor

Choice of materials and finishes used in the interior design of the area must take into account the structural and maintenance considerations listed under site facilities at the end of this section. Paint for example, should not chalk, powder, or flake, to avoid unwanted dust.

The finish of the Honeywell equipment is durable, attractive, and easy to maintain. The devices are *black* and *white* with colored accent panels. Standard accent color is blue; red and yellow panels are available for an extra charge with a Request for Price Quotation (RPQ) from the Marketing Sales Representative. Table 8-4 lists standard and optional equipment colors.

Space Requirements

The floor area required is determined by the system's complement of equipment. Also, the system's floor space depends upon the shape of room, the number and locations of permanent walls, partitions, entrances and exits.

Storage facilities for media and other items necessary for system operation should be designed to minimize both the amount of area necessary and travel time between areas.

Consider the possibility of later expansion when you are selecting an area.

Clearance

Specific considerations involved in designing an efficient processing center vary from installation to installation. Five major considerations for space and specifications, however, apply:

- Do not underestimate growth potential. The trend is toward additional minicomputer uses, and this means additional equipment and, in turn, additional space.
- Make sure that the equipment is situated where Honeywell recommends (see page 8-11A) for the best operation and comfort.
- Deviations from the recommended environmental specifications (included in this section) can cause serious problems in the operation and maintenance of equipment.
- Power isolation and regulation are necessities particularly since growth in the amount of power may be required.
- Space for expansion must be allotted for at least one expansion cabinet.

Operation and Peripherals

Honeywell has determined the optimum minisystem arrangement of equipment at a site, based on efficient operation. Specific criteria include:

- The console is the center of operations. The operator while sitting at the console can swing left, right, or back and be able to easily access equipment from all the usual working locations.
- Aisles to and from system at least 92 cm (36") wide allow access to all peripherals,

TABLE 8-4. EQUIPMENT COLORS

Color	Manufacturers Chip Number	Honeywell Standard Chip Number		Honeywell Standard and Optional Accent Colors
		Aspect	Tab #	
Gothic Black		Spatter	003	
		Smooth	252	
Executive White		Spatter	703	Standard Colors
		Smooth	704	
Black Laminate	Nevamar LH-6-1 (L)	Leather	601	
White Laminate	Formica White 949	Smooth	600	
Caribbean Blue		Spatter	001	
		Smooth	250	
Hunter Red		Spatter	004	Optional Accent Colors
		Smooth	254	
Aztec Yellow		Spatter	005	
		Smooth	254	

media supplies, and any maintenance equipment that must fit through the aisles.

- The freestanding peripherals should be arranged according to the frequency of operator access.
- The displays of module devices, freestanding cabinets, and add-on peripherals should be visible from the console.

After evaluating the possible areas, you should prepare 1:50 cm (1/4″ to 1′) equipment layouts for areas under consideration. Use the scaled template in this section (page 8-30) for this purpose. Page 8-11 indicates a maximum system layout accompanied by complete specifications (Table 8-6) and followed by a photograph to be used as an overall guide.

The site layout should show:

- Entries and exits from truck off loading point
- Adjacent corridors, ramps, and staircases
- Building columns and internal windows.
- Site storage and media storage areas
- Any under-floor or above-floor obstructions that affect installation or routing of interconnecting cables.
- Raceways at walkways (when used)
- Ac ground
- Ac load centers
- System ground point
- Communication terminals (if used)

The final layout must be approved by you, by the Marketing Representative and by Field Engineering.

Air Conditioning (If required)

Minicomputer equipment, like any other equipment that consumes electrical energy, produces heat. As a result, air conditioning is an important requirement in site planning. This is not just for personnel comfort; the equipment media and system media can tolerate conditions only within certain limits. Temperature regulation, humidity control, and air filtration are all essential factors for the system. The central processor, rackmountable devices, and freestanding peripherals are internally cooled by blowers that circulate room air through louvers in the cabinetry.

Air intake and exhaust varies slightly from one device to another. In general, cool air is transferred through louvers from front to rear, side to side, along the bottom edge (in some units) and lower pan section of cabinet where cables enter the devices. For proper regulation of the environment of the computer room, air conditioning is required.

Any required air conditioning system for the installation should be completely separate and completely automatic, regulating conditions measured at the equipment air intake within the following range:

System Environmental Requirements		
	Operating Conditions	Storage Conditions
Temperature (dry bulb)	16°C to 32°C (60°F to 90°F)	5°C to 43°C (40°C to 110°F)
Rate of Change/hr	±5.6°C (10°F)	
Relative Humidity	30% to 60% (No Condensation)	10% to 80% (No Condensation)
Rate of Change/hr	10%	
Atmospheric Pressure	562 mm Hg (16.88 in.) to 780 mm Hg (30.71 in.)	
Rate of Pressure Change/min	60 mm Hg (2.4 in./min)	

The lower limit for relative humidity depends on the characteristics of the cards, disk packs, and paper to be used; on personnel comfort; and on the need to eliminate static electricity. The upper limit is subject to the condition that no condensation form on the equipment.

To maintain operating conditions within these limits, Honeywell recommends design conditions of:

Temperature (dry bulb)	24°C (75°F) ±8.4°C (±15°F)
Relative Humidity	45%

The individual environmental specification for the CPS9450, CPS9460, and CPS9461 Central Processors and their associated attached memory when used within a RETMA cabinet, separate rack, or an enclosure (by customer) is as follows:

Central Processor and Memory Environmental Requirements		
	Operating Conditions	Storage Conditions
Temperature (dry bulb)	10°C to 50°C (50°F to 122°F)	5°C to 45°C (41°F to 113°F)
Rate of Change/hr	±5.6°C (10°F)	
Relative Humidity	5% to 95% (No Condensation)	95%

design and not tied too closely to the proposed arrangement of the computer. In this way later changes can be effected without disruption of computer opeation. In essence, the aim should be to condition the room and not the minicomputer.

After the system is installed and operating, the air supply dampers must be adjusted to balance the temperature throughout the area. Take care to locate and eliminate hot spots. It is suggested that an independent firm specializing in air balancing be employed to balance the computer room and provide certified test results to Honey-

In large facilities containing more than two systems, different design-point temperatures may exist in remote points of the room. This causes no problem as long as the temperature does not change more than ±5.6°C (±10°F) at any one measurement point.

In determining the air conditioning requirements of your installation, consider:

1. The types of equipment that will be dissipating heat in the confined space. The central system and peripheral devices are cooled by air circulating fans that pull room air into the cabinet and exhaust the warmed air, usually out through the top or sides.
2. The heat gain and air conditioning loss through walls, ceilings, windows, doors, partitions, and lighting.

To find the number of tons of air conditioning required when kcal/hr (or Btu/hr) is known, use the formula:

$$\frac{kcal}{1000} \ or \ \frac{Btu/hr}{12,000} = tons \ of \ air \ conditioning$$

Continuous monitoring of the site's temperature and humidity is recommended as a way to save downtime. Recording instruments will indicate, for example, the extent and duration of any undesirable environmental conditions. The recorder used should satisfy the following criteria:

● The means of delivering air to the minicomputer area should not be tied too closely to the proposed layout of the equipment, in case of changes later. Flexibility can be achieved by using dampers and louvers to control the quantity and direction of air flow or by using a ventilated ceiling with certain panels masked off.

● Distribution of air to any other conditioned areas can be conventional, but the supply of air from the main air conditioner will need reheating if used directly. Small areas such as equipment and media storage areas can be conditioned by spillover air from the computer room, entering through suitable grilles or a doorway and then extracted back to the main air conditioners.

Air filtration is an essential adjunct to the regular cleaning regime to help ensure continuous and reliable operation of Level 6 systems.

To make the filtration system effective, seal all windows and control smoking in the area. In addition, provide for outdoor clothing to be removed and stored outside the area. Exert control on the supplier of continuous paper to leave only a minimum amount of loose paper dust adhering to the pack. The paper itself should not lose filler readily when it is handled.

This specification requirement serves for a *stand-alone environment only* for the central processor and memory during operation, storage, and shipping.

The individual environment specification requirements regarding the table-top and free-standing devices are listed below, followed by the device environment requirements.

Model Types	Description
o TWU9101	Keyboard Typewriter Console
o DIU9101 and DIU9102	Single and Dual Diskettes
o CDU9101 through CDU9104	Cartridge Disk
o CRU9101 through CRU9104	Card Readers
o PRU9101 and PRU9102	Serial Printers
o PRU9103 through PRU9106	Line Printers

Individual Device Environmental Requirements

	Operating Conditions	Shipping Conditions
Temperature (dry bulb)	10°C to 38°C (50°F to 100°F)	5°C to 45°C (41°F to 113°F)
Rate of Change/hr	±5.6°C (10°F)	
Relative Humidity	10% to 90% (No Condensation)	95%
Rate of Change/hr	5%	
Atmospheric Pressure	562 mm Hg (21.41 in.) to 780 mm Hg (30.71 in.)	
Rate of Pressure Change/min	60 mm Hg (2.4 in./min)	

NOTE: Wider humidity variations are allowable in some cases under a more restricted temperature range.

Paper Media Environmental Requirements

	Operating Conditions	Storage and Shipping Conditions
Temperature (dry bulb)	10°C to 38°C (50°F to 100°F)	5°C to 45°C (41°F to 113°F)
Rate of Change/hr	11°C (20°F)	
Relative Humidity	30% to 70% (No Condensation)	95%
Rate of Change/hr	5%	
Atmospheric Pressure	562 mm Hg (16.88 in.) to 780 mm Hg (30.71 in.)	
Rate of Pressure Change/min	60 mm Hg (2.4 in./min)	

Three additional factors to consider are discussed below:

1. Humidity control will improve the performance of paper-handling devices (card readers, etc.), eliminate static electricity, and avoid condensation and moisture. (The walls of the computer room should be adequately vapor sealed to reduce moisture problems.)

2. Filtration may be necessary in all areas to ensure clean air for the continuous and reliable operation of the minisystem.
There are many sources of dirt, both from outside (clothes, shoes, dandruff, as well as the air supply) and within the room (magnetic oxide and paper dust produced by handling these materials on the system itself). However, provided the precautions are taken, the recommended standard of filtration, operating on the major source of dirt, has been found to ensure the satisfactory operation of card readers, printers and disk devices, and other sensitive devices, in association with the standard routine for cleaning these devices individually. It is relatively simple to filter the air to a good standard — a standard admittedly higher than the ultimate cleanliness of the room is likely to reflect — but it is not considered economic to go to extreme lengths in attempting to control the controllable sources of dirt when several uncontrollable sources still exist.

3. Air distribution, the means of delivering air to the computer room, should be flexible in

Types of Systems

Whether you choose an overhead room air supply, an underfloor plenum supply, a combination system, or a freestanding air conditioner, you should use an experienced air conditioning engineer or consulting firm before designing the conditioning system. These specialists can assess the requirements for your installation. Window air conditioning units are not recommended because they are designed mainly for summer, not year-round cooling.

Electrical Power

You must furnish and install primary power for the system in accordance with the system specifications in Figure 8-7. It is also your responsibility to furnish and install the electrical equipment for the installation, including fittings, distribution panel, the raised floor device cutouts (if required), and transformer and voltage regulator (if required). Future expansion should always be considered, as provision for extra power facilities saves added installation costs later.

Many of the problems associated with computer operations originate in the primary ac power system. Disturbances such as electrical noise, power interruptions, and lightning must be factored into the plans for the power system for the user to have reasonable assurance that the computer system will perform satisfactorily and continue to operate. Close coordination with the electrical utility representative can lead to correction of potential problems originating in the utility system supplying power to the building. Many of the services and disturbances that can seriously affect an operation, however, are generated within the building itself. Your plant engineer, the electrical utility engineer, together must identify these disturbances and take steps to prevent possible adverse effects on the operation of the minisystem.

Power Source

The power source must have sufficient capacity to handle present computer loads and any loads likely to be imposed by future expansion of the system. The source must be independent of all other loads. That is, it must not provide power

Figure 8-7. Schematic Showing Wye-Connection, Voltage, and Receptacle Relationship For PDU

for airconditioning equipment, convenience outlets, lighting, or office equipment. A separate building service entrance (or a main building service panel) input feeder connected to the computer distribution panel usually provides suitable power (see Figure 8-7).

To obtain isolation, if needed, a separate transformer and service drop is required to provide power to the computer system. The transformer must be adequate to handle the present load plus any future expansion. Many large buildings have multiple power systems with numerous service entrances supplied from the same transformer. An isolation transformer must be used to reduce noise and transient interference if you intend to connect to the available power.

The power that serves the system must meet the following requirements:

- The line voltage should not have voltage transients greater than +6% or -14% from the nominal line to neutral of 120 volts.

- The line voltage should have total harmonic content of less than 6% of the power in the fundamental frequency.
- The line voltage must not have neutral grounded at any point in the entire power system supplying the computer except at the building service entrance or at isolation transformer when applicapable.
- The PDU power source must be 120/208 volts, three-phase +10%-15% of the rated voltage, with a frequency tolerance of 60 Hz ±1/2 Hz and with a harmonic content within acceptable limits.

Ac Power Sources for Types CPS9450, CPS9460 and CPS9461 Systems

Each cabinet contains a power distribution unit (PDU) (see page 8-8) located at the bottom front of the cabinet when Central Processor (CP), Control Panel, Memory Save, and second Console ASR are figured in system complement. Each PDU requires its own connection to the primary power source (ac mains). A 6-foot power cable is attached to the rear of each PDU.

TABLE 8-5. RECEPTACLE SPECIFICATIONS

Type	Symbols	Amps	Volts	Phase and Wires	Mfg.	NEMA Std.	Unit Plug No.	Receptacle by Customer Or	Connector by Customer
A	Ⓐ	30	600	3∅-5W	Hubbell or Arrow – Hart		25415	25403	25414
F	Ⓕ	15	125	1∅-3W	Hubbell	5-15P	5266C	5262	5269

NOTE

The receptacle specifications are for your convenience. Refer to the manufacturer's catalog for complete compatibility as to exact equivalent. Honeywell assumes no responsibility for differences between manufacturers' receptacles.

The system is arranged so that energizing the power switch on the central processor drawer causes all outlets throughout the system to be energized, provided that the circuit breaker on each PDU is "on."

NOTE: De-energizing the circuit breaker in any cabinet removes power in that cabinet and all subsequent cabinets.

The permissible primary power to the Type CAB9003 system cabinet sources are as follows (permissible power sources for free-standing peripheral devices are described in Table 8-5.)

Ac power requirements – either of the following sources may be utilized:

1. Input voltage could be from a 208 VAC RMS, 60 Hz, 2-phase, 3-wire, plus ground source with 24A at 208 VAC RMS.
2. 230/240/250 VAC RMS center-tapped (neutral) 60 Hz, single-phase, 3-wire, plus ground source. In either case, the Hubbell 25414 or 25403 (customer supplied) must be wired with the high lines connected to pins X and Y and the neutral center tap connected to pin W.

Loading on the input lines will be from phase to neutral on two phases only. Maximum load current per phase will be 24A; there is no internal provision or procedure for balancing the load. The unused phase is truncated at the input connector. The cabinet containing the central processor requires a drop; the second cabinet (options) is slave to the central processor cabinet. If a third cabinet is required, another drop is used. The fourth cabinet, if required, is slaved to the third. All cabinets requiring drops receive a "primary power contactor pick" voltage from the central processor cabinet.

The voltage shall be firm, varying by not more than ±10% of the rated amount, including transient and steady state. Where power is not regulated this closely, you are advised to furnish and install a voltage regulator.

Your Honeywell Marketing Representative or Field Engineer will answer your questions, but for redesign or highly technical problems, you should contact your electrical contractor or consulting engineering firm.

Power Distribution

If the electric power for the PDU at the installation site is *not* of the required voltage, one or more transformers must be purchased and installed. A three-phase transformer or equivalent of identical rating and characteristics can be used. The capacity required depends upon the equipment complement and what is specified in the calculated installation specification.

The total system requires a power load balance calculation only when single-phase devices are included in the equipment. It is your responsibility to ensure that the phase loads are balanced (i.e., that the amperage is distributed evenly among the three phases of the system's power source). Load balancing prevents a large load from occurring on one phase of the transformer.

In a three-phase, wye-connected system with a grounded neutral, the phase imbalance currents flow in the neutral wire. This reduces the power system's efficiency, increasing power consumption and operating costs. High neutral ground currents can also generate noise levels that may be reflected back into the computer system. To avoid these problems, attention must be given to balancing the computer load throughout the system.

The feeder supplying power to the computer system should be protected by a mainline circuit breaker. The computer's distribution power panel should be located in an unobstructed, well-lighted area in the computer room.

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Convenience Outlets

Auxiliary power, 120-volt, single-phase, 60-Hz wall outlets must be present in the computer area for the service engineers scopes, test equipment etc., vacuum cleaner, floor buffer, etc. Recommended circuit capacities are 15-20 amperes; individual outlet capacities are 15 amperes. The number and location of these outlets should be indicated on your approved system layout drawing. All convenience outlets in the computer room should be on a feeder separate from the computer system to prevent electrical noise interference.

Grounding

When providing the female receptacle or connectors for three-phase and single-phase devices, furnish and install a separate ground wire. Conduit, raceway, or other enclosures cannot be used for this purpose. For three-phase power, the fifth wire is to be used as the equipment ground; for single phase, the third wire. In both cases, the ground shall be connected to the metallic raceway system and/or the control panel, in accordance with the National Electrical Code (NFPA) No. 70.[1] The equipment ground shall *not* be connected to the neutral wire except at the building's main electrical service entrance. The ground wire, when installed in armor, cable sheath, conduit raceway, ladder tray, or other enclosure, should be sized according to the amperage specified in Table 250-95 of the National Electrical Code.[1] In no case shall it be smaller than number 12AWG.

WARNING

A power distribution unit five-wire connection (four-wire wye plus equipment ground) is used in Honeywell systems; the neutral is readily available. The neutral supplied is usually the white conductor in a multiconductor power cable.

The ac neutral must not be confused with protective (equipment frame) ground. The protective equipment ground — the green conductor in a multiconductor cable prevents the buildup of dangerous voltages on equipment as protection for personnel. It ensures that any short circuit between a power phase and the cabinet draws enough current to trip the circuit's protective device immediately — rather than raising the potential of the equipment to a dangerous level. The ac neutral must never be connected to the frame of any equipment or to the protective ground.

Interconnecting Cables

Honeywell supplies and installs the necessary cables and raceway (if used) for the initial instal-

[1] National Fire Protection Association, 470 Atlantic Avenue, Boston, MA 02210

lation of the computer (with the exception of the ac cables). Since all cables are custom-made to specific lengths (see Table 8-6) it is essential that an approved system layout drawing be available at the proper time.

Any revisions of approved system layout drawings are considered on an RPQ (Request for Price Quotation) basis because a second cable order must be prepared.

Cables required for new, additional, or damaged equipment through the fault of Honeywell and within warranty period are supplied by Honeywell at no cost.

If cables are requested in other than standard lengths, the new cable lengths and the reason for the change must be specified on a Request Price Quote (RPQ) basis.

Power Receptacles and Connectors

You are required to install power receptacles and/or connectors in accordance with local electrical codes before delivery of the system. The locations and types of ac receptacles are given in Table 8-5 for each device. For quick reference in estimating a power load, the electrical specifications for each device are included in the summary table at the beginning of the section. The power loads listed do not represent the duty cycle, nor have they been derated to indicate the duty cycle. To meet the NFPA 70 Electrical Code, the primary distribution must be sized by the nameplate rating specified on the device.

The values shown for circuit breakers and wire sizes must also meet the NFPA 70 Code. Follow your local code if it requires larger sizes. The wires shown include the required "green wire" or safety ground conductor.

For a summary of receptacle specifications, see Table 8-5.

Figures 8-8 through 8-10 illustrate the ac-type male plugs that can be attached to the computer devices or to the power panel (depending on its location). The dimensions indicated for the connectors and receptacles are overall measurements and can be used in calculating subfloor clearances and clearances in walkways, cable channels, and raised floor cutouts.

Device Specifications

Models 6/34 and 6/36 consist of the following installation specifications for a system and are based on the individual device specifications in Table 8-6. If any devices or modules are added or deleted, the associated specifications should be revised by the customer, with copies sent to your Honeywell Marketing Representative. In this way, both the customer and Honeywell will have first-hand information for reworking total system requirements.

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NO. 25415
SYMBOL Ⓐ
TYPE A

Figure 8-8. Power Plug — Three-Phase, 30-Amp,
Five-Wire, 600V
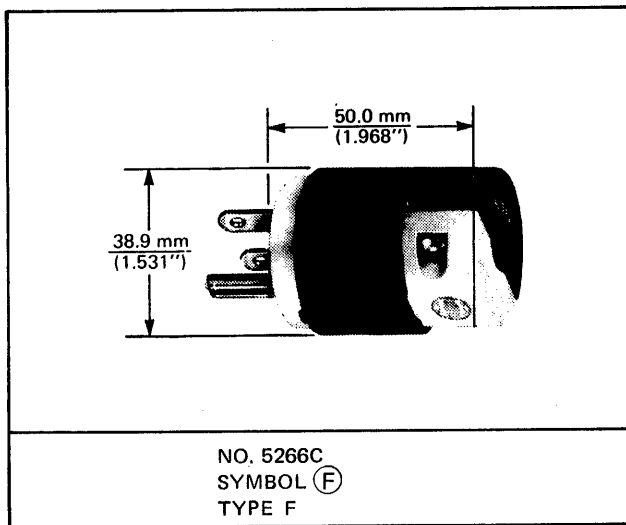

NO. 5266C
SYMBOL Ⓕ
TYPE F

Figure 8-9. Power Plug — Single-Phase, 15-Amp,
Three-Wire, 125V

TABLE 8-6. CENTRAL PROCESSING SYSTEM SPECIFICATIONS

Marketing Identifier	Description	Electrical Power				Heat Gain kcal/hr or Watts (Btu/hr)	Dimensions W/D/H cm (in.)	Weight kg (lb.)	Cables (max.) m (ft.)	
		KVA	Amps	Type	Symbol				ac	dc
CPS9450 CPS9460 CPS9461	**Cabinet 1:** Central Proc. 64K Memory also includes CP cabinet fully loaded with power chassis and devices.	See Notes a and b	1/30	A	Ⓐ	2016 or 2343[b] (8,000)	52.0/76.2/156.2 (20.5/30/61.5) With control panel overhang: xxx/92.2/xxxx (xxx/36.25/xxx)	226[b] (500)	1.8 (6)	15.2 (50)
CAB9010	Extension – Table Wing	–	–	–	–	–	60.9/76.2/76.2 (24/30/30)	29.9 (66)	–	–
CPS9450 CPF9403	**6/34 Control Panel** (CP rackmountable) or (CP Tabletop CAB9001)	0.41	1/15	F	Ⓕ c	403 or 645 (1,600)	50.5/77.9/16.25[d] (19.9/30.7/6.4)	29.4 (65)	1.8 (6)	15.2 (50)
CPS9460/ CPS9461 CPF9403	**6/36 Control Panel** (CPU rackmount-able) or (CPU Tabletop CAB9001)	0.41	1/15	F	Ⓕ c	403 or 645 (1,600)	50.5/77.9/16.25[d] (19.9/30.7/6.4)	29.4 (65)	1.8 (6)	15.2 (50)

CONSOLE SPECIFICATIONS

Marketing Identifier	Description	KVA	Amps	Type	Symbol	Heat Gain	Dimensions	Weight	ac	dc
TTU9101	ASR-33 Teleprinter	0.26	1/15	F	Ⓕ c	94 or 109 (375)	55.8/46.9/66 (22/18.5/26)	25.4 (56)	1.8 (6)	7.6 (25)
TTU9102	KSR-33 Teleprinter	0.23	1/15	F	Ⓒ c	94 or 109 (325)	55.8/46.9/66 (22/18.5/26)	25.4 (56)	1.8 (6)	7.6 (25)
TWU9101	Keyboard Typewriter	0.23	1/15	F	Ⓕ	126 or 156 (500)	57.15/52.07/19.05 (22.5/26.5/13.1)	31.7 (70)	1.8 (6)	15.2 (50)
DKU9101	CRT (TTY)	0.10	1/15	F	Ⓕ	252 or 292 (1,000)	20.3/60.9/33.0 (18/24/13)	18.1 (40)	1.8 (6)	15.2 (50)
	Keyboard	–	–	–	–	N/A within CRT (N/A within CRT)	20.3/20.3/7.6 (18/8/3)	N/A within CRT (N/A within CRT)	N/A	Allow 0.9m (3 ft.) Separation

DISKETTES SPECIFICATIONS

Marketing Identifier	Description	KVA	Amps	Type	Symbol	Heat Gain	Dimensions	Weight	ac	dc
DIU9101	Single Diskette (rackmountable or tabletop unit)	0.42	1/15	F	Ⓕ c	85 or 100 (340)	52.07/68.3/18.5[d] (20.5/26.9/7.3)	27.2 (60)	1.8 (6)	6 (20)
DIU9102	Dual Diskette (rackmountable or tabletop unit)	0.84	1/15	F	Ⓕ c	171 or 199 (680)	52.07/68.3/37[d] (20.5/26.9/14.6)	54.4 (120)	1.8 (6)	6 (20)
PSS9001 PSS9002	**Memory Save and Autorestart** (rackmountable) or (tabletop)	0.42	1/15	F	Ⓕ c	72 or 84 (285)	44.7/59.9/8.8[d] (17.6/23.6/3.5)	22.7 (50)	1.8 (6)	10.7 (35)

CARTRIDGE DISK SPECIFICATIONS

Marketing Identifier	Description	KVA	Amps	Type	Symbol	Heat Gain	Dimensions	Weight	ac	dc
CDU 9101 through CDU9104	Cartridge Disk Units	0.80	1/15	F	Ⓕ e	290 or 337 (1,150)	48.2/76.2/24 (19/30/8.75)	38.6 (85)	2.4 (8)	3.3 (11)

Honeywell

– TYPICAL SYSTEM ELECTRICAL REQUIREMENTS –

GENERAL:

A. Ac power and electrical ground source will be supplied by the customer based on the requirements listed in these specifications.

B. The electrical power source should be independent and isolated from all other loads, where applicable.

C. An allowance for expansion is recommended. (See Sheet 2 for specifications.)

D. All wiring must be installed in accordance with the National Electrical Code and other local ordinances. Costs for installing and/or modifying will be borne by the customer.

REQUIREMENTS:

A. The customer will supply and install all ac receptacles indicated in the system layout and in Table 8-6 for individual unit specifications.

B. Ac power requirements for Level 6 Systems central processor cabinet with power distribution unit (PDU) and expansion cabinets (add-ons). Any of the following sources may be utilized:

   1. Input voltage could be from a 208 VAC RMS, 60 Hz, two-phase, 3-wire, plus ground source with 24A at 208 VAC RMS, or

   2. 230/240/250 VAC RMS center-tapped (neutral) 60 Hz, single-phased, 3-wire, plus ground source. In either case, the Hubbell 25414 or 25403 (customer supplied) must be wired with the high lines ("hot" wires) connected to pins X and Y and the neutral center tap connected to pin W.

   3. Loading on the input lines will be from phase to neutral on two phases only. Maximum load current per phase will be 24A; there is no internal provision or procedure for balancing the load. The unused phase when three phase is used, is truncated at the input to the RF1 filter in the PDU. Cabinet containing central processor requires a drop; second cabinet (options) is slave to central processor cabinet. If third cabinet is required, another drop and PDU are used. Fourth cabinet, if required, is slaved to third. All cabinets requiring drops receive a "primary power contactor pick" voltage from central processor cabinet. No growth factor is required.

C. Listed below are the electrical specifications for the Level 6 System and devices:

Central Processor Cabinet and ASR33 Teletypewriter

Load –

Voltage – 120/208 ±10%

Frequency – 60 Hz ±1/2 Hz

Phase and number of wires as indicated.

Load – 0.85 kVA

Voltage – 120 $^{+10\%}_{-15\%}$

Frequency – 60 Hz ±1/2 Hz

Phase and number of wires as indicated.

NOTE: The equipment neutral wire must not be connected to building ground except at power source (transformer, or building service entrance).

In the unusual cases in which the power company does not regulate its power within the above tolerances and/or your facility imposes heavy loads on their substations, you are advised to furnish and install a voltage regulator.

Interconnecting cables between units shall be protected from mechanical injury. Product line raceways can be purchased through your Honeywell sales representative if raised flooring is not used. Raceway specifications are available from your Honeywell Sales Representative. The cost of supplying and installing raceway will be borne by the customer.

Figure 8-13. Installation Specification Format (Sheet 1)

– TYPICAL SYSTEM ENVIRONMENTAL REQUIREMENTS –

GENERAL:

A. The heat dissipation figures listed on Sheet 2 for each unit *do not include* the heat gain from other sources: namely, lighting, people, building transmission, and fresh air loads. The total, however, allows for a 30% growth in equipment and should be considered when figuring the size of the air conditioning system.

B. Check NFPA-75 for fire protection information.

C. Costs for installing and/or modifying air conditioning will be borne by the customer.

REQUIREMENTS:

A. Listed below are the environmental specifications.

1. Cooling required for equipment only _____ kcal/hr or _____ watts (_____ Btu/hr or _____ tons).

2. Temperature measured at input air of minisystem units – 24°C ±-8.4°C (75°F ±15°F).
   Rate of change/hr – ±-5.6°C (10°F/hr). (No condensation.)

3. Relative humidity – 30 to 60%

4. Filtration – Normal, unless environment is subjected to corrosive gases, salt air, or other unusual conditions, in which case special filtering will be required. If mechanical filters are used, their efficiency rating shall not be less than 20%.

5. It is strongly recommended that any required air conditioning system be a separate system because year-round cooling is required. (Window-type air conditioning units are not recommended.)

REFERENCES:

For additional information and recommendations concerning the above subjects, as well as acoustical ceilings, fire control, cables, etc., contact your local Honeywell Sales Representative or Field Engineer.

Figure 8-13 (cont). Installation Specification Format (Sheet 2)

Qty.	Device	Marketing Identifier	Electrical Power (kVA)	Receptacles (amps/symbol/type)	Heat Gain (kcal/hr or watts)	Weight (kg)	Dimensions W/D/H (cm)	Cables (m)	
								ac	dc
Total									
30% Growth Factor									
GRAND TOTAL									

Figure 8-13 (cont). Installation Specification Format (Sheet 3)

Qty.	Device	Marketing Identifier	Electrical Power (kVA)	Receptacles (amps/symbol/type)	Heat Gain (Btu/hr)	Weight (lbs)	Dimensions W/D/H (in)	Cables (ft)	
								ac	dc
Total									
30% Growth Factor									
GRAND TOTAL									

Figure 8-13 (cont). Installation Specification Format (Sheet 4)

LEGEND

+	Casters
●	Levelers
◆	Level and lock casters
F	Front of unit
------	Clearance
▨	Unit cutout
▩	Power panel (by customer)
━■━	Operators Extension Table Support
▬	Control panel
■	Legs and casters (casters are replaced by levelers)
⑮	Raceway callout
A Ⓐ F Ⓕ	Receptacle supplied and installed by customer (when specified)

Figure 8-14. Floor Layout Grid
Scale: 1:50mm (1/4 in.)

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